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STUDY AND MODELING OF NANOSCALE GCGS DG MOSFET

« Étude et modélisation du transistor GCGS DG MOSFET nanométrique »

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By

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2. T. Bentrcia**,** F. Djeffal, M.A. Abdi, M. Chahdi & N. Boukhennoufa, ″An Accurate Two Dimensional Threshold Voltage Model for Nanoscale GCGS DG MOSFET Including Traps Effects″, *3rd International Conference on Signals, Circuits and Systems SCS'2009, (CD), pp. 273-277, Djerba, Tunisia, November 06-08, 2009 (Available also at IEEE Xplore).*

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4. T. Bentrcia, F. Djeffal and A. Benhaya, ″Continuous Analytic I-V Model for GS DG MOSFETs Including Hot-Carrier Degradation Effects″, submitted to Electronics Letters.

Book Chapter

1. T. Bentrcia and F. Djeffal, ″Compact Modeling of Multi-Gate MOSFET Including Hot-carrier Effects″, Chapter 4, CMOS Technology, Series: Electrical Engineering Developments, Editor: Min-jun Kwon, Nova Science Publishers, ISBN: 978-1-61761-325-8, NY, USA, 2010.

INTRODUCTION

Advances in semiconductor manufacturing techniques and ever increasing demand for faster and more complex Integrated Circuits (ICs) have driven the associated Metal Oxide Semiconductor Field Effect Transistor (MOSFET) sizes close to their physical limits. On the other hand, it has not been possible to scale the supply voltage used to operate these ICs proportionately due to factors such as compatibility with previous generation circuits, noise margin, power and delay requirements, and non-scaling of threshold voltage, subthreshold slope, and parasitic capacitance [1]. While the consequent increase in internal electric fields in aggressively scaled MOSFETs comes with the additional benefit of increased carrier velocities, and hence increased switching speed, it also presents a major reliability problem for the long term operation of these devices. As devices are scaled the benefits of higher electric fields saturate while the associated reliability problems get worse.

The presence of mobile carriers in the oxides triggers various physical processes that can drastically change the device characteristics during normal operation over prolonged periods of time eventually causing the circuit to fail. Such degradation in device and circuit behavior due to injection of energetic carriers from the silicon substrate into the surrounding dielectrics is known as “hot-carrier degradation” [2].

It is clear that the presence of large electric fields has major influence on the long term operation of modern ICs. These Hot-Carrier (HC) related device instabilities have become a major reliability concern in modern Metal Oxide Semiconductor (MOS) transistors and are expected to get worse in future generation of devices. The study of the fundamental physical processes that result in device parameter variation due to HC injection is essential to provide guidelines for avoiding such problems in future ICs.

In the past, methods for the evaluation of HC reliability have been based on physical models for long-channel transistors. These approaches have been remarkably successful in predicting the time-dependence of HC degradation on factors such as channel length, channel doping, and supply voltage in long-channel devices. Even though the limitations in their application to deep sub-micron devices have long been recognized, as devices are scaled, the same techniques continue to be applied to short-channel devices. In short-channel devices,

however, several assumptions made in the conventional approaches break down and hence the parameters associated with most of these models lose their physical meaning. These model parameter are usually extracted by fitting the model to experimental data. Such empirical approaches, though useful for qualitative evaluation of existing technologies, provide little insight into the physical mechanisms responsible for the device degradation. Furthermore, the semi-physical model parameters extracted from a given set of experiments on a particular technology are not able to predict the device behavior under process modifications essential to meet circuit performance requirements as the devices are scaled. Hence such approaches cannot be used for predictive modeling and/or to aid the semiconductor industry in designing manufacturing processes to overcome the relevant reliability problems. The presence of novel physical mechanisms such as short-channel effects, non-local carrier heating, and quantum effects in aggressively scaled devices further complicates the modeling process and requires the use of more comprehensive modeling techniques for such structures [3].

This thesis is structured in four chapters divided into two parts: the state of the art and contributions. The state of the art part presents background on MOSFET structure particularly when scaled to deep submicron level, hence many unwanted phenomena altering the correct function of the device. The contribution part contains our proposals for modeling the performance of deep submicron MOSFET devices including the hot-carrier degradation effects when compared to the conventional bulk devices.

The thesis presents a study of the degradation of proposed MOSFET device parameters, which affect circuit operation, due to processes initiated by injection of high energy carriers into the gate oxide, the characterization techniques used to measure and attribute these parameter shifts to the underlying processes, and the use of empirical, semi-empirical, and physical models to predict the time dependence of the parameter degradation during circuit operation. The current understanding of the basic concepts related to MOSFET devices is presented in Chapter I. This chapter highlights the processes that need to be modeled in device simulation tools in order to be applicable to predictive simulation of HC phenomena in current and future generation MOSFETs.

Chapter II and onwards start our contributions. In Chapter II we describe the development of modeling tools along with the choices and assumptions that were made to model the physical mechanism described in Chapter III in a practical simulation application. The details of the numerical model developed as a result of this analysis in subthreshold region are presented.

The results of the application of these simulation tools to HC degradation in GS DG MOSFET for both linear and saturation regimes are presented in Chapter IV.

Finally, we conclude this thesis and present our view on future research directions.

Chapter I

DEEP SUBMICRON MOSFETS

Abstract: The compact modeling of MOS transistors for integrated circuit design has, for many years, been driven by the needs of digital circuit simulation. Conventional bulk CMOS technology is still prevalent in the microelectronics industry. According to the International Technology Roadmap for Semiconductors, bulk MOS transistors will still be used for the 45 nm technology node (gate length around 18 nm), which is expected to be running by 2010. The feasibility of 15 nm conventional MOS transistors in bulk CMOS technology has already been demonstrated.

The purpose of this chapter is to provide both an overview about the evolution of MOSFETs devices in addition to the basic physics theory required to build compact models required later for the deduction of some mandatory parameters and for the incorporation of new constraints in the function of the device.

I.1. INTRODUCTION

Since the 60's the shrinking of electronic components has been driven by the fabrication of integrated circuits, which will continue for at least the next two decades. The critical feature size of the elementary devices (physical gate length of the transistors) will drop from 25 nm in 2007 (65 nm technology node) to 5 nm in 2020 (14 nm technology node). In the sub-10 nm range, beyond--CMOS (complementary MOS) devices will certainly play an important role and could be integrated on CMOS platforms in order to pursue integration down to nm structures. Si will remain the main semiconductor material in a foreseeable future, but the needed performance improvements for the end of the ITRS (international technology roadmap for semiconductors) will lead to a substantial enlargement of the number of materials, technologies and device architectures [4].

Therefore, new generations of nanoelectronic integrated circuits (ICs) present increasingly formidable multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, etc.) resulting in an urgent need of long term research based on a scientific approach, in order to understand the underlying physical mechanisms and hence remove the present technological limitations. The industry is indeed increasingly relying on new ideas in order to continue technological innovation [5].

This chapter addresses the basic concepts related to the MOSFET technology, with some advanced ideas for keeping CMOS on the road. Different regimes characterizing the function of a MOSFET device are also depicted, in addition to some challenging problems encountering the downscaling process and their associated solutions. This chapter can be considered as an introductory platform for further chapters.

I.2. EVOLUTION OF CMOS TECHNOLOGY

As the density of integrated circuits continues to increase, a resulting shrinkage of the dimensions of the individual devices of which they are comprised has followed. Smaller circuit dimensions reduce the overall circuit area, thus allowing for more transistors on a single die without negatively impacting the cost of manufacturing. However, this reduction in device size is only one of three factors identified by Moore in the increased density of modern integrated circuits. Equally important are the two other factors of an increase of die size and an increase in circuit cleverness - the reduction in number of devices and chip area to implement a given circuit or function. All of these lead to the driving force for continued

integration complexity is the reduction in cost per function for the chip as indicated by figure Fig.I.1 [6].

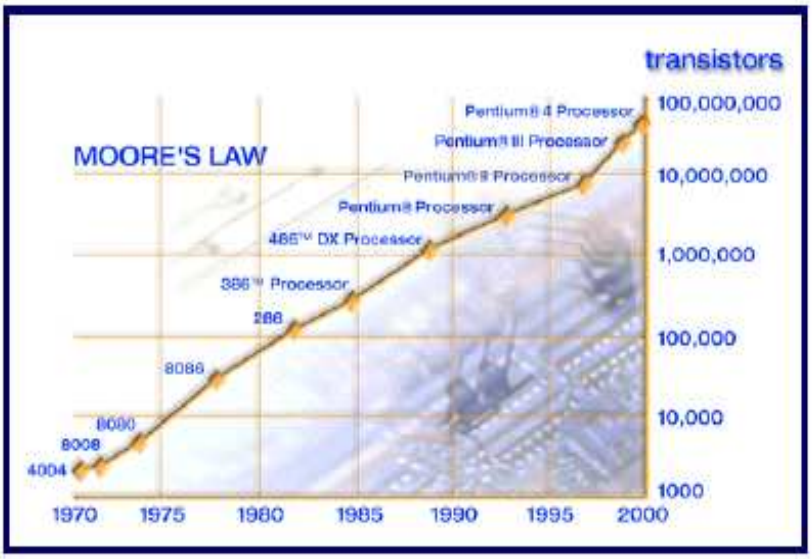


Fig. I.1. Moore's Law predictions for devices scaling [6].

As semiconductor feature sizes shrink into the nanometer scale regime, device behavior becomes increasingly complicated as new physical phenomena at short dimensions occur, and limitations in material properties are reached. In addition to the problems related to the actual operation of ultra-small devices, the reduced feature sizes require more complicated and time-consuming manufacturing processes. This fact signifies that a pure trial-and-error approach to device optimization will become impossible since it is both too time consuming and too expensive. Nevertheless, it is important to consider these new physical effects which will occur in small devices, as these effects may well eventually dominate device performance.

The traditional scaling of classical planar CMOS devices leads to performance limitations, which have to be overcome by introduction of new device architectures. New so-called 'non-classical' CMOS device concepts are being developed. A development roadmap of CMOS device architectures is shown in Fig. I.2 in comparison with standard bulk devices. Some of these advanced device structures will probably be introduced within the next 5–10 years. The ultimate CMOS device with the multi-gate FET structure will potentially carry the silicon technology down to below 10 nm feature sizes, but it is also challenged by process complexity and manufacturability; its key advantages are, lithography independent gate length control and higher drive currents [7].

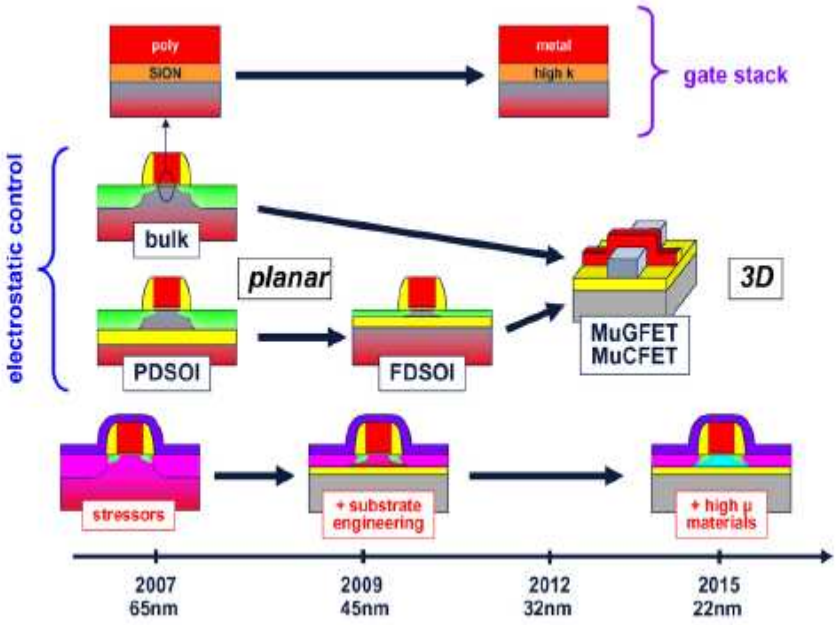


Fig. I.2. Simplified transistor roadmap (courtesy ENIAC) [7].

I.3. MOSFET STRUCTURE AND OPERATION

I.3.1. Presentation of the Structure

As the name metal-oxide-semiconductor (MOS) suggests, the MOS transistor consists of a semiconductor substrate (usually silicon) on which is grown a thin layer of insulating oxide (SiO) of thickness t_{ox}. A conducting layer (a metal or heavily doped polysilicon) called the gate electrode is deposited on top of the oxide. Two heavily doped regions of depth X_j, called the source and the drain are formed in the substrate on either side of the gate. The source and the drain regions overlap slightly with the gate (see Fig. I.3.) [8].

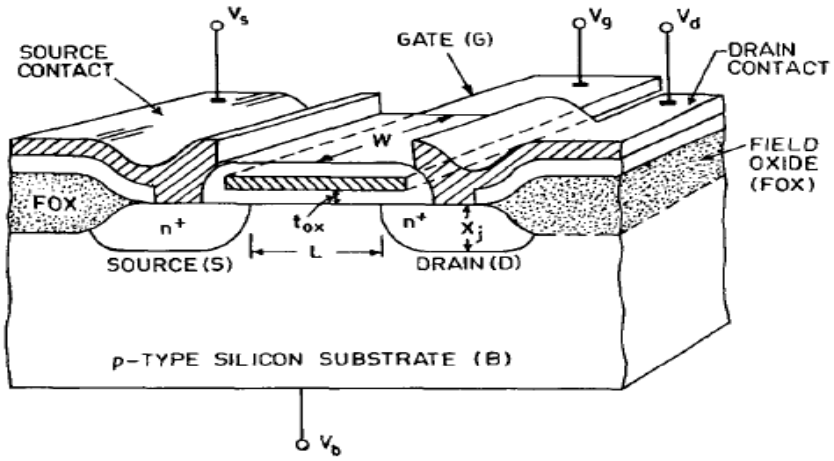


Fig. I.3. MOS transistor structure showing three-dimensional view [8].

The source-to-drain electrodes are equivalent to two p-n junctions back to back. This region between the source and drain junctions is called the channel region. Thus a MOS transistor is essentially a MOS structure, called the MOS capacitor, with two p-n junctions on either side of the gate. The field oxide (FOX) shown in Figure I.3. is for isolating various devices on the same substrate. From the circuit model point of view, a MOS transistor is a four terminal device, the four terminals are designated as gate g, source s, drain d, and substrate or bulk b. Note that the structure is symmetrical. Because of this symmetry one cannot distinguish between the source and drain of an unbiased device; the roles of the source and the drain are defined only after the terminal voltages are applied.

Under normal operating conditions, a voltage *V,* applied to the gate terminal creates an electric field that controls the flow of the charge carriers in the channel region between the source and the drain. Since the device current is controlled by the electric field (vertical field due to the gate voltage and lateral field due to the source to drain voltage) the device is known as a MOS Field-Effect-Transistor (MOSFET). Because the gate is electrically isolated from the other electrodes, this device is also called an Insulated-Gate Field-Effect Transistor (IGFET). Another acronym sometime used is MOST for the MOS Transistor. The bulk of the semiconductor region, shown as substrate in Figure I.3, is normally inactive, since the current flow is confined to a thin channel at the surface of the semiconductor. It is for this reason the substrate region is also referred to as the body or bulk of the MOSFET.

MOSFETs may be either n-channel or p-channel depending upon the type of the carriers in the channel region. An n-channel MOS transistor (nMOST) has heavily doped *n+* source and drain regions with a p-type substrate and has electrons as the carriers in the channel region.

I.3.2. Operation Modes

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. In the following discussion, a simplified algebraic model is used that is accurate only for old technology. Modern MOSFET characteristics require computer models that have rather more complex behavior.

For an enhancement-mode, n-channel MOSFET, the three operational modes are [9]:

Subthreshold, or weak-inversion mode ($V_{GS} < V_{th}$),where V_{th} is the threshold voltage of the device: According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source. In reality, the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a subthreshold current that is an exponential function of gate–source voltage. While the current between drain and source should ideally be zero when the

transistor is being used as a turned-off switch, there is a weak-inversion current, sometimes called subthreshold leakage.

In weak inversion the current varies exponentially with gate-to-source bias V_{GS} as given approximately by:

$$I_D \approx I_{D0} e^{\frac{V_{GS}-V_{th}}{nV_T}} \tag{I.1}$$

where I_{D0} is the current at $V_{GS} = V_{th}$ and the slope factor n is given by $n = 1 + C_D / C_{OX}$, with C_D is the capacitance of the depletion layer and C_{OX} is the capacitance of the oxide layer. In a long-channel device, there is no drain voltage dependence of the current once $V_{DS} >> V_T$, but as channel length is reduced drain-induced barrier lowering introduces drain voltage dependence that depends in a complex way upon the device geometry (for example, the channel doping, the junction doping and so on). Frequently, threshold voltage V_{th} for this mode is defined as the gate voltage at which a selected value of current I_{D0} occurs, for example, I_{D0} = 1 μA, which may not be the same V_{th}-value used in the equations for the following modes.

Some micropower analog circuits are designed to take advantage of subthreshold conduction. By working in the weak-inversion region, the MOSFETs in these circuits deliver the highest possible transconductance-to-current ratio, namely: $g_m / I_D = 1 / (nV_T)$, almost that of a bipolar transistor.

The subthreshold *I–V curve* depends exponentially upon threshold voltage, introducing a strong dependence on any manufacturing variation that affects threshold voltage; for example: variations in oxide thickness, junction depth, or body doping that change the degree of drain-induced barrier lowering. The resulting sensitivity to fabricational variations complicates optimization for leakage and performance.

Linear region also known as the ohmic mode ***($V_{GS} > V_{th}$*** and ***$V_{DS} < (V_{GS} - V_{th})$***

The transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages as shown in figure Fig. I.4. The current from drain to source is modeled as:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{I.2}$$

where μ_n is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{ox} is the gate oxide capacitance per unit area. The transition from the exponential subthreshold region to the triode region is not as sharp as the equations suggest.

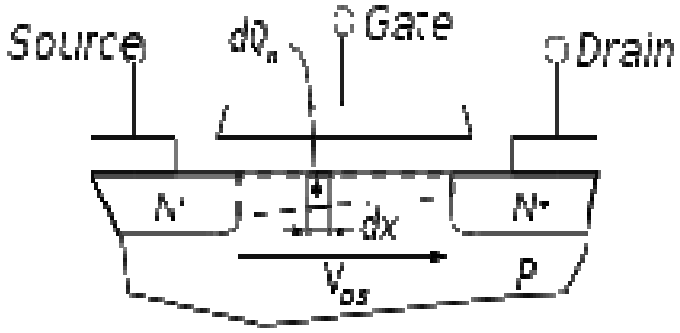


Fig. I.4. Cross section of a MOSFET operating in the linear (Ohmic) region;
strong inversion region present even near drain.

Saturation or active mode ($V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$)

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as pinch-off to indicate the lack of channel region near the drain (Fig.I.5). The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modeled very approximately as:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{I.3}$$

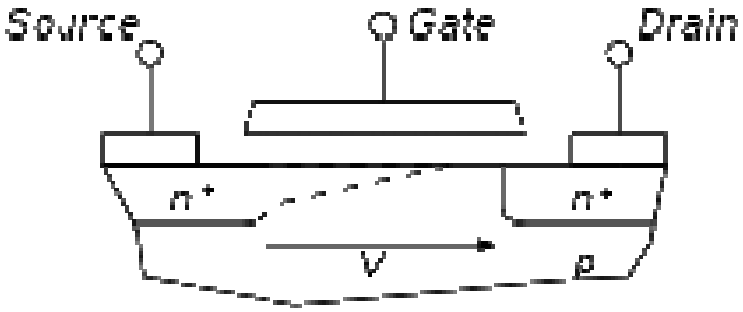


Fig. I.5. Cross section of a MOSFET operating in the saturation (active) region;
channel exhibits pinch-off near drain.

The boundary between linear (Ohmic) and saturation (active) modes is indicated by the upward curving parabola in figure Fig. I.6.

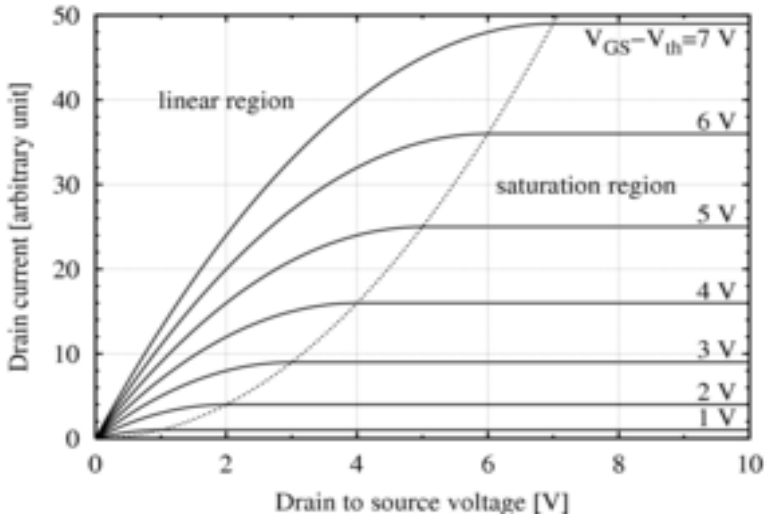


Fig. I.6. MOSFET drain current vs. drain-to-source voltage for several values of $V_{GS} - V_{th}$.

As the channel length becomes very short, these equations become quite inaccurate. New physical effects arise. For example, carrier transport in the active mode may become limited by velocity saturation. When velocity saturation dominates, the saturation drain current is more nearly linear than quadratic in V_{GS}. At even shorter lengths, carriers transport with near zero scattering, known as quasi-ballistic transport. In addition, the output current is affected by drain-induced barrier lowering of the threshold voltage.

I.4. SMALL SIGNAL PARAMETERS

These parameters are required for the small-signal analysis. In addition they are also required for linearizing nonlinear drain current models. The output conductance and transconductance, are important parameters in analog circuit design, these parameters can easily be derived from the device drain current model [10]. Under normal operation, a voltage applied to the gate, drain or substrate results in a change in the drain current. The ratio of change in the drain current I_{ds} to the change in the gate voltage V_{gs} while keeping drain voltage V_{ds} and substrate voltage V_{bs} constant is called transconductance expressed as:

$$g_m = \left.\frac{\Delta I_{ds}}{\Delta V_{gs}}\right|_{V_{ds},V_{bs}} \tag{I.4}$$

The transconductance is one of the important device parameters as it is a measure of device gain. Thus, the gain of a MOSFET can be increased by:

- Increasing C_{ox}, that is, using a MOSFET with a thinner gate oxide (lower t_{ox}),

- Using devices with higher carrier mobility μ**.** Since μ of the electrons is higher than that of holes, an nMOST has higher gain compared to pMOST.
- Using devices with larger channel width *W* and shorter channel length *L*. While decreasing *L*, scaling considerations must be taken into account.

Since g_m, is sensitive to the quality of the gate oxide (through μ and V_{th} parameters), it is frequently used to monitor the effect of hot-carrier stress and accelerated aging on device reliability.

In addition to g_m**,** the MOSFET has two other conductances. The ratio of change in the drain current due to change in V_{bs} for a fixed V_{gs}, and V_{ds}**,** is called substrate transconductance g_{mbs} defined as:

$$g_{mbs} = \left.\frac{\Delta I_{ds}}{\Delta V_{bs}}\right|_{V_{gs},V_{ds}} \tag{I.5}$$

Finally, the ratio of change in the drain current to the change in the drain voltage V_{ds} is called drain conductance or simply conductance gds given similarly by:

$$g_{ds} = \left.\frac{\Delta I_{ds}}{\Delta V_{ds}}\right|_{V_{gs},V_{bs}} \tag{I.6}$$

Figure I.7 shows plot of g_m, g_{mbs} and g_{ds} as a function of V_{gs} and V_{ds}, based on first order MOSFET model.

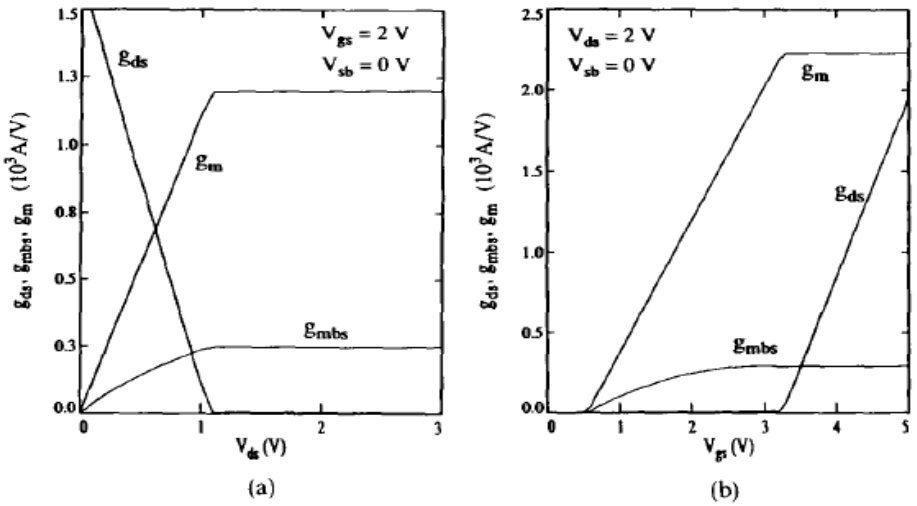


Fig. I.7. Small-signal parameters g_m, g_{mbs} and g_{ds} as a function of (a) V_{ds}, and (b) V_{gs},.

If all the voltages are changed simultaneously, then the corresponding total change in the drain current is:

$$\Delta I_{ds} = \frac{\partial I_{ds}}{\partial V_{gs}} \Delta V_{gs} + \frac{\partial I_{ds}}{\partial V_{ds}} \Delta V_{ds} + \frac{\partial I_{ds}}{\partial V_{bs}} \Delta V_{bs} = g_m \Delta V_{gs} + g_{ds} \Delta V_{ds} + g_{mbs} \Delta V_{bs} \quad \text{(I.7)}$$

If the change in the voltages is small, approaching zero, then these (trans)conductances are called small signal (trans)conductances. The small signal equivalent circuit of a MOSFET is shown in Figure I.8, where rhomic symbols represents controlled current sources.

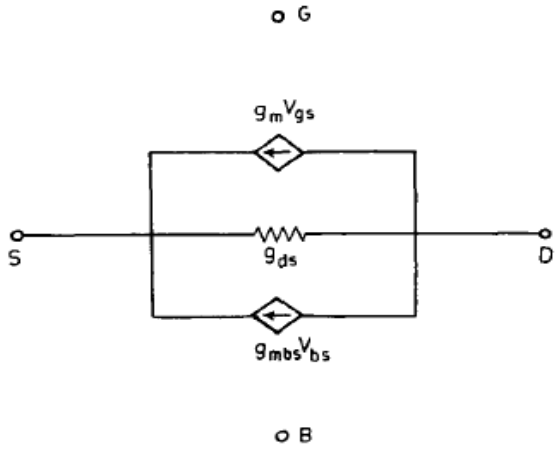


Fig. I.8. A low frequency, usually less than 1 KHz, small-signal model for a MOSFET.

I.5. MINIATURIZATION EFFECTS

Producing MOSFETs with channel lengths much smaller than a micrometer is a challenge, and the difficulties of semiconductor device fabrication are always a limiting factor in advancing integrated circuit technology. In recent years, the small size of the MOSFET, below a few tens of nanometers, has created operational problems [11].

- *Higher subthreshold conduction*

As MOSFET geometries shrink, the voltage that can be applied to the gate must be reduced to maintain reliability. To maintain performance, the threshold voltage of the MOSFET has to be reduced as well. As threshold voltage is reduced, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available; the circuit design is a compromise between strong current in the "on" case and low current in the "off" case, and the application determines whether to favor one over the other. Subthreshold leakage (including subthreshold conduction, gate-oxide leakage and reverse-biased junction leakage), which was ignored in the past, now can consume upwards of half of the total power consumption of modern high-performance VLSI chips.

- *Increased gate-oxide leakage*

The gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance when the transistor is on and to reduce subthreshold leakage when the transistor is off. However, with current gate oxides with a thickness of around 1.2 nm (which in silicon is ~5 atoms thick) the quantum mechanical phenomenon of electron tunneling occurs between the gate and channel, leading to increased power consumption.

Insulators (referred to as high-k dielectrics) that have a larger dielectric constant than silicon dioxide, such as group IVb metal silicates e.g. hafnium and zirconium silicates and oxides are being used to reduce the gate leakage from the 45 nanometer technology node onwards. Increasing the dielectric constant of the gate dielectric allows a thicker layer while maintaining a high capacitance (capacitance is proportional to dielectric constant and inversely proportional to dielectric thickness). All else equal, a higher dielectric thickness reduces the quantum tunneling current through the dielectric between the gate and the channel. On the other hand, the barrier height of the new gate insulator is an important consideration; the difference in conduction band energy between the semiconductor and the dielectric (and the corresponding difference in valence band energy) also affects leakage current level. For the traditional gate oxide, silicon dioxide, the former barrier is approximately 8 eV. For many alternative dielectrics the value is significantly lower, tending to increase the tunneling current, somewhat negating the advantage of higher dielectric constant.

- *Increased junction leakage*

To make devices smaller, junction design has become more complex, leading to higher doping levels, shallower junctions, "halo" doping and so forth, all to decrease drain-induced barrier lowering. To keep these complex junctions in place, the annealing steps formerly used to remove damage and electrically active defects must be curtailed increasing junction leakage. Heavier doping is also associated with thinner depletion layers and more recombination centers that result in increased leakage current, even without lattice damage.

- *Lower output resistance*

For analog operation, good gain requires a high MOSFET output impedance, which is to say, the MOSFET current should vary only slightly with the applied drain-to-source voltage. As devices are made smaller, the influence of the drain competes more successfully with that of the gate due to the growing proximity of these two electrodes, increasing the sensitivity of the MOSFET current to the drain voltage. To counteract the resulting decrease in output

resistance, circuits are made more complex, either by requiring more devices, for example the cascade and cascade amplifiers, or by feedback circuitry using operational amplifiers, for example a circuit like that in the adjacent figure Fig. I.9, where the operational amplifier provides feedback that maintains a high output resistance.

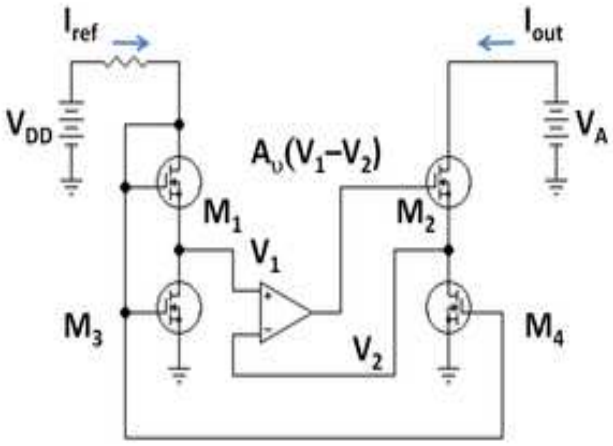


Fig. I.9. MOSFET version of gain-boosted current mirror; M_1 and M_2 are in active mode, while M_3 and M_4 are in Ohmic mode, and act like resistors.

- *Lower transconductance*

The transconductance of the MOSFET decides its gain and is proportional to hole or electron mobility (depending on device type), at least for low drain voltages. As MOSFET size is reduced, the fields in the channel increase and the dopant impurity levels increase. Both changes reduce the carrier mobility, and hence the transconductance. As channel lengths are reduced without proportional reduction in drain voltage, raising the electric field in the channel, the result is velocity saturation of the carriers, limiting the current and the transconductance.

- *Interconnect capacitance*

Traditionally, switching time was roughly proportional to the gate capacitance of gates. However, with transistors becoming smaller and more transistors being placed on the chip, interconnect capacitance (the capacitance of the wires connecting different parts of the chip) is becoming a large percentage of capacitance. Signals have to travel through the interconnect, which leads to increased delay and lower performance.

- *Heat production*

The ever-increasing density of MOSFETs on an integrated circuit creates problems of substantial localized heat generation that can impair circuit operation. Circuits operate slower at high temperatures, and have reduced reliability and shorter lifetimes. Heat sinks and other cooling methods are now required for many integrated circuits including microprocessors.

Power MOSFETs are at risk of thermal runaway. As their on-state resistance rises with temperature, if the load is approximately a constant-current load then the power loss rises correspondingly, generating further heat. When the heat sink is not able to keep the temperature low enough, the junction temperature may rise quickly and uncontrollably, resulting in destruction of the device. In order to assist designers in the device selection process, a simulation tool can be used to simulate in-circuit performance.

- *Modeling challenges*

Modern ICs are computer-simulated with the goal of obtaining working circuits from the very first manufactured lot. As devices are miniaturized, the complexity of the processing makes it difficult to predict exactly what the final devices look like, and modeling of physical processes becomes more challenging as well. In addition, microscopic variations in structure due simply to the probabilistic nature of atomic processes require statistical predictions. These factors combine to make adequate simulation and "right the first time" manufacture difficult.

I.6. EMERGENT SOLUTIONS

Many solutions have been proposed in literature among them we have [12],

I.6.1. High-k and metal gate integration

Low-power applications such as battery operated handheld devices require a reduced gate leakage current. To reduce the gate leakage, standard oxynitride gate insulators will be replaced by high-*k* dielectrics. Among the promising candidates for the 45 nm technology node are hafnium oxides (HfO_2) and hafnium silicates HfSiON with a high-*k* value in the range 10–15, which should be compared to 3.9 for SiO_2 and 6–7 for the oxynitrides. This leads to significantly reduced gate leakage for the same equivalent oxide thickness. The main issues related to these types of dielectric materials, which still have to be addressed by researchers, are the high number of fixed/trapped charges and interface states. Both threshold voltage stability and low-field mobility are negatively affected by the high amount of charge present in the high-*k* oxides.

While the reduced mobility can be partially offset by strain enhancement techniques, the poor threshold voltage control and possible reliability problems cannot be accepted. An additional complication is the poor thermal stability of high-*k* materials. The dielectrics should be stable during high temperature processing steps (mainly source/drain activation anneals), since, e.g., recrystallization can increase the gate leakage current. For the ultimate scaling of CMOS, below 10 nm gate length, other high-*k* materials such as La_2O_3, with a larger *k* value might be of interest. The choice of suitable materials is limited by the additional constraint that the band gap offset should be large enough compared to silicon. In some cases the offset to either the conduction or valence band is too small. By considering the increased fringing field, due to the higher *k* value, the influence on short channel effects and switching speed can be analyzed to find an optimum *k* value close to 30.

High-*k* materials are often used in combination with different metal gate electrodes, e.g., TiN, TaN. Metal gates are important for several reasons, including the ability to control threshold voltage by tuning the work function of the gate electrode. For nitrided metal gates the tuning can be done either during the reactive sputter deposition or by subsequent nitrogen ion implantation. This allows reduced channel doping and hence higher mobility in both bulk and thin body SOI devices. Furthermore, metal gates do not suffer from depletion, compared to the case with a highly doped polysilicon gate electrode. For successful metal gate integration, selective etching processes, with high anisotropy, need to be developed for patterning of 10nm gate lengths. The use of fully nickel silicided (FUSI) polysilicon gates offers a more straightforward approach in this respect, since the patterning of polysilicon gates is more mature. In this case, the work function control can be achieved by dopant pile-up at the metal gate/oxide interface. The combinationof FUSI and high-*k* has generated a lot of attention recently.

I.6.2. Strain-enhanced mobility

For high-performance applications the challenge is mainly to maintain sufficiently high drive current for short-channel devices which suffer from short channel effects and high parasitic resistances. For higher drive current and increased switching speed the focus is on different methods of mobility enhancement, using strain. For CMOS applications both higher hole and electron mobility are desired. For PMOS the first attempts at increased channel mobility were done by selective SiGe epitaxy in the channel region. However, from the 90 nm technology node, selective SiGe growth in the source/drain has emerged as the preferred method to create compressive strain in the PMOS channel. Significantly increased electron mobility has also been demonstrated in NMOS devices, where a dielectric capping layer, commonly silicon

nitride, introduces a tensile strain in the channel region. In this approach the strain in both PMOS and NMOS channels becomes uniaxial, which is beneficial compared to biaxial strain. It is important to note that the NMOS and PMOS can be optimized independently of each other. Very high mobility can also be achieved for both electrons and holes using so called virtual substrates, with a thin Si-channel on top of a relaxed SiGe buffer layer. There are several issues with the virtual substrate technique, including a poor thermal conductivity and a high intentional concentration of defects (dislocations). Furthermore the mobility increase is smaller for holes, which is not advantageous for CMOS applications, where the PMOS has the most need for performance increase.

I.6.3. Multi-gate devices

Multi-gate MOSFETs realized on thin films are the most promising devices for the ultimate integration of MOS structures due to the volume inversion in the conductive layer, leading to an increase in the number and the mobility of electrons and holes. The on-current *I*on of the MOSFET is limited to a maximum value *I*BL that is reached in the ballistic transport regime. For a given DIBL, an increased ballisticity is obtained for low doping double gate SOI devices. The transfer characteristics of several multiple-gate (1, 2, 3 and 4 gates) MOSFETs, calculated using the 3D SchrÄodinger{Poisson equation and the non equilibrium Green function (NGEF) formalism for the ballistic transport or MC simulations, have shown similar trends. The best performance (drain current, subthreshold swing) is outlined for the 4-gates (QG | quadruple gate or GAA | gate all around) structure. However, the propagation delay in triple gate (TG) and quadruple gate MOSFETs are degraded due to a strong rise of the gate capacitance. A properly designed double-gate (DG) structure appears to be the best compromise at given current (For a double gate device, the impact of a gate misalignment on the drain current is important. The impact of a gate misalignment is significant for *I*on in 2G MOSFETs. A large back gate (BG) shift reduces the saturation current compared to the aligned case, whereas a slight BG shift towards the source increases *I*on. This is due to a lower source access resistance. In terms of short channel effects, aligned transistors exhibit the best control while highly misaligned MOSFETs operate like single gate ones. The current is much more influenced by the misalignment than *I*on due to a degradation of the electrostatic control. The oversized transistor shows attractive static performance and a larger tolerance to misalignment but the dynamic performance is rapidly degraded as the overlap length increases.

In decananometer MOSFETs, gate underlap is also a promising solution in order to reduce the DIBL effect. The on-current is almost not affected by the gate underlap whereas the leakage

currents are substantially reduced due to a decrease in DIBL and drain to gate tunneling current. A reduction of the effective gate capacitance *C*g for larger underlap values at *I*on has also been shown. This reduction of *C*g leads to a decrease in the propagation delay and power. In order to reach very high performance devices at the end of the roadmap, multi-bridge-channel MOSFETs (MBCFET) present very high driving currents larger than those of GAA devices and exceeding the ITRS requirements as given by figure Fig. I.10.

Fig. I.10. Schematic diagram of MBCFET on SOI [12].

The main advantage of multi-gate devices is their excellent electrostatic control of the channel, which reduces the short channel effects. On the other hand, since the conduction takes place in a volume instead of just one surface, these devices present higher mobility than conventional bulk MOSFETs because there is less scattering; their operation can even be near the ballistic limit for very short channel devices.

In multiple gate devices, the use of a very thin film allows to downscale the devices without the need of using high channel doping densities and gradients. In fact, undoped films can be used: the full depletion of the thin film prevents punch-through from happening. Besides, the absence of dopant atoms in the channel increases the mobility by suppressing impurity scattering. On the other hand, unwanted dispersion of the characteristics is avoided; this dispersion results from the random microscopic fluctuations in ultra-small devices.

Multiple gate nanoscale devices have many advantages in circuit performance. A very high packaging density is possible because of the small size of these devices, caused by the short channel and the thin film. Because of the higher mobility, transconductance can be higher, which gives more current gain and allows a higher operating frequency. Therefore, multiple gate nanoscale devices have a big potential for RF and microwave applications. The analog

performance is also very good. Voltage gain is much higher than in conventional bulk MOSFETs, and especially in moderate inversion: the reduction of short channel effects leads to a higher Early voltage, and on the other hand the g_m/I_{ds} characteristics have higher values than in conventional MOSFETs [13]. Regarding digital applications, the small subthreshold swing of multiple gate devices keeps a high ratio between on current and off current even for devices with channel lengths of the order of nm.

I.7. NANOTECHNOLOGIES

The nanoelectronics platforms, bear a striking resemblance to the good old-fashioned silicon microelectronics, in that exploit the electrical and magnetic properties if fairly simple materials. All of the approaches discussed to date have also reached a point in their commercialization, where we can be reasonably certain that something will come of them [14]. Molectronics (sometimes called “moletronics”) is different, because it has a lot further to go commercially. In fact, it isn’t even all that well-defined. Indeed, molectronics is basically a catchall term for electronics that uses complex (often biological) molecules as the main materials platform. There is a considerable amount of interesting R&D in this field that is being performed in both academic and industrial laboratories that involves quantum computing or chemical computing, although this kind of molectronics is so far off in terms of commercialization, that we can so no real business opportunities emerging from this work in this decade. Instead, this kind of thing will remain in university labs or in the labs of the very largest electronics and semiconductor firms for many years to come. There is another aspect to molectronics, though, one that is closer to commercialization, and which researchers believe will present some genuine opportunities in the next five to ten years. This approach is one in which switching is based upon the change in state of individual molecules. The change can be based on conductivity as a result of an applied field (much like a classical FET), a conformational change resulting in a change of conductivity (including a complete contact break) or optical properties. In practice, devices may contain many such molecules in an individual switching unit. Although some approaches to this kind of molectronics involve radical changes in circuit design, others are more in line with conventional architectures.

All this diversity—no settled materials, designs, or architectures—is symptomatic of the early stage of development at which molectronics currently exists. Probably the closest product to commercialization that might be classified as molectronics is a memory chip from a firm called Zettacore, which uses complex molecules as material platform, but otherwise doesn’t

diverge too much from standard chip designs. However, when looking further into the future, when processors and logic may be built using molectronics, molectronics will probably require significant changes in approach to design largely as a result of having to build in a fairly high level of fault tolerance [15].

Now it may be the turn of nanophotonics to add its contribution. A number of start-ups have opened their doors in this space and the European Union has just launched a large R&D program focused on exactly this area. The impact of nanophotonics is fairly diverse. NanOpto makes a range of nanoengineered polarizers, splitters, and "waveplates," using a nanoimprint lithography. Toshiba has claimed a breakthrough when it recently announced quantum dot light sources that could transmit single photons and this type of device would most probably be used in quantum encryption. It seems more likely that the first big business for nanoengineered lasers will come from chip interconnection. Until recently, the speed bottleneck in computing and telecom was the speed of the processors. In the last few years, however, the processor speed has reached a point at which it is the interconnections that are now the limiting factor. In response, semiconductor manufacturers have moved from aluminium interconnects to copper interconnects and are now experimenting with optical interconnection as well as exotic lower-k materials and carbon nanotubes. Optical interconnection could supply more than enough bandwidth to suck up and supply data to even the fastest processors. The requirements for lasers to support such an application would very demanding in terms of size and cost, but the market size is potentially huge. For on-chip applications, the lasers would have to be embedded and their value would be subsumed by that of the entire chip. But an examination of the on-board market suggests that addressable markets for nano-engineered interconnects could be huge. Consider a board with 10 devices on it. If these devices were fully interconnected, 90 lasers would be required [16].

I.8. CONCLUSION

The multi-gate devices that control the channel from multiple sides and very thin body devices are new to circuit and system designers. These devices need to be modeled to understand and predict the functionality of the circuits. Compact device models are used in circuit design. New compact models that accurately model these novel devices, and are computationally efficient, are in development. There are new physical effects that now need to be incorporated into these device models.

The use of multiple gate devices in circuit design is critically dependent on the availability of accurate models for these devices. Using appropriate models, circuit simulation allows to

design circuits with devices of adequate dimensions. Circuit simulation requires accurate models of the current and the terminal charges of the devices in addition to the modeling of additional constraints.

Chapter II –

DEFECTS IN MOSFET DEVICES

Abstract: The hot-carrier effect is a reliability problem which occurs when hot (energetic) carriers cause Si-SiO, interface damage and/or oxide trapping. This leads to the degradation of the current drive capability of the transistor, thus eventually causing circuit failure. The origin of this degradation is the high electric field near the drain end. One of the most effective ways to control the hot-carrier effect is to include a field reducing region in the transistor structure. These regions, called the LDD (lightly doped drain) or MDD (moderately doped drain), reduce the amount of damage a device suffers, and consequently increase its operational lifetime.

This chapter is dedicated to the description of the main defects occurring in MOSFETs structure due to intrinsic anomalies or stress conditions, the hot-carrier degradation shift on the main parameters is also studied and the basic models used for the modelling of such phenomenon are presented.

II.1. INTRODUCTION

A global view of today's world permits to notify that many hardware and software based systems, are characterized by complex behavior and often have special features and structures requiring high complexity approaches for modeling [17]. In such situation, this may result in many unwanted phenomena disturbing the correct function particularly when taking into account the VLSI constraints. In order to avoid the heavy costs associated with maintenance and diagnostic operations, a deep understanding of the degradation process should be established so that the reliability of such systems can be enhanced significantly. Despite that the recent progress in different fields has made resulted products more powerful than ever, the increasing level of complexity implied that reliability problems not only will continue to exist, but also are likely to require ever more innovative solutions [18].

The demand for high-performance devices has been experiencing a steady rise in the sophistication degree of semiconductor manufacturing techniques, which in turn have driven the associated MOSFET size close to their physical limits. Theoretical analyses make it clear that we should be able to rearrange atoms and molecules one by one to get more efficient tools at a tiny scale. Therefore, the initial stage consists in the seek of new design approaches for devices miniaturization scheme, the adopted approach based on keeping the internal electric fields constant had to be abandoned due to several practical reasons including [19]:

- Loss of compatibility with previous generation circuits,
- Decrease in noise margins because of the non-scaling of the threshold voltage and the subthreshold slope,
- Decrease in operating speeds in sub-micron devices due to the non-scaling of parasitic capacitances.

In this chapter, our aim is to present different types of defects that can exist in MOSFET devices, these defects are a major concern in reliability field. Therefore, their inclusion in compact models can bring deep understanding towards the resolution of many problems for integrated circuit design. The shift caused by the phenomenon in some basic parameters is also studied and the basic models used for the modeling of the hot-carrier degradation effects are presented.

II.2. DEFECTS CLASSIFICATION

In spite of the effort paid up to now by the scientific community concerning Silicon and silicon based devices widely used in many fields of physics, there still remain a lot of aspects not clarified, related to the behavior of impurities, and a global understanding of their local structure and properties became increasingly important due to the reduction in chip sizes and to the increase of the operation speed [20].

Since the reliability concepts are the most popular framework allowing the good description of the system life cycle based on failures occurrence; which is mainly caused by the original existence or generation of defects in the device, it would be of great utility to analyze different evolution stages. The reliability of semiconductor devices is represented by the failure rate curve known as the “bathtub curve”, depicted in figure II.1. The curve can be divided into three regions [21]:

- Initial failures are considered to occur when a latent defect is formed, then becomes manifest under the stress of operation. Generally, the period of initial failures is defined as the first six months to one year of a product cycle, the failure rate tends to decrease with time because only devices having latent defects will fail, and these devices are gradually removed.
- Random failures in which the failure rate is constant, such mode covers soft errors, electrical noise, electrostatic discharge, and other problems. All of these problems will occur at random under the stress of external factors.
- Wear-out failures occur due to the ageing of devices from wear and fatigue. This period indicates the life of different failure modes of semiconductors such as Hot carriers, electromigration and time dependant dielectric breakdown.

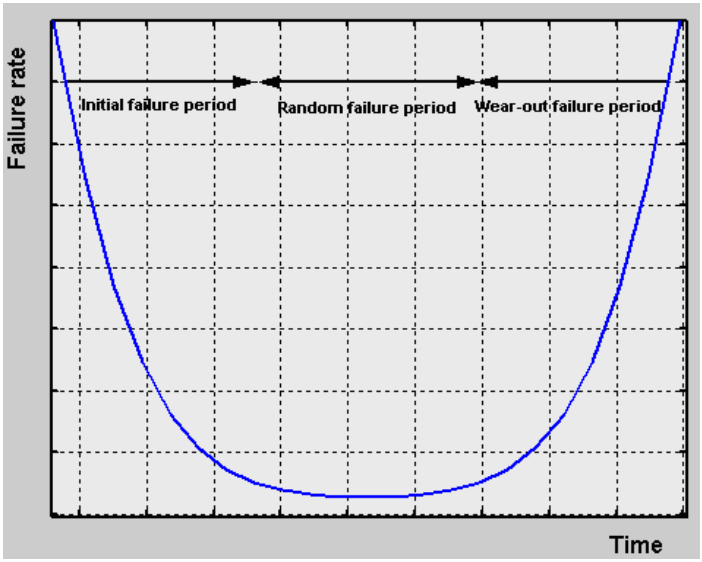


Fig. II.1. Failure rate curve (Bathtub Curve) of semiconductors devices.

In the screening process, if we assume a certain length of time (t_0) before device shipment, the lifetime can be forecasted by the probability density function. With the Weibull distribution density function [22], the rate of accumulated failures (t: t_0) available after screening becomes:

$$F(t_0 : t) = 1 - \exp\left(-\frac{(t_0 + t)^m - t_0^m}{\eta^m}\right) \quad \text{(II.1)}$$

where m and η are scale and shape parameters of the Weibull distribution.

Therefore, it's possible to estimate the device lifetime basing on probabilistic exploitation of such distribution density function. The reliability based analysis highlights the necessity to improve the device lifetime through the enlargement of the random failures interval, where the failure rate is approximately constant. Hence, it's a mandatory requirement to assimilate existing defects in both extreme regions, so that abusive effects could be eliminated or at least reduced [23].

II.2.1. Bulk defects

This type of defects is closely related to the bulk structure of a semiconductor, in the sense that the trap defects are distributed over the whole volume. The resulted effect on the behavior of future produced devices has been studied intensively in literature. However, with the advance of MOSFETs technology at nanoscale level, the gap becomes more apparent and additional efforts then before should be focused on the subject.

Origin of the problem

The availability of semiconductor materials and their use as a basis of nanodevices have bring to the front many disadvantages related from a part to the inherit structure and from another part to production process constraints. In single crystal semiconductors, deep level used impurities have usually a metallic nature, but they can be crystal imperfections (dislocations, precipitates, vacancies, and interstitials) [24]. Such defects are in general avoidable, but occasionally they are intentionally introduced to affect a device characteristic (switching time, resistivity). For amorphous semiconductors, defects are mainly due to structural imperfections. Manufacturing environment conditions are also a key medium altering the concentration of existing impurities in the semiconductor; methods used for crystal growth such as epitaxy can give rise to deep level traps. Another recognized cause concerns several properties of employed resources; the higher static charge levels in a semiconductor fab than in a conventional room. In fact, it is not uncommon for a fab with no safeguards against static charge to achieve levels of tens of kilovolts on a variety of critical surfaces.

The existence of foreign atoms or crystal defects perturbs the periodicity of the single crystal, hence resulting in discrete energy levels into the band gap, as illustrated in figure II.2. They can be considered as recombination centers when there are excess carriers, and as generation centers when the carrier density is below its equilibrium value.

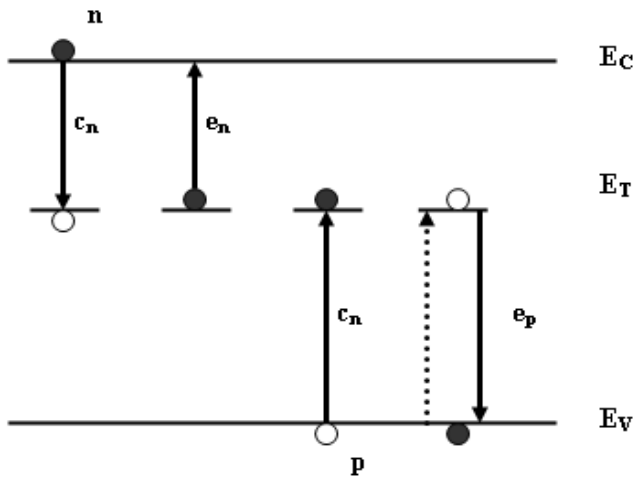


Fig. II.2. Electron energy band diagram for a semiconductor with deep-level impurities in addition to capture and emission process.

The thermodynamics of defects plays an important role in the deduction of some specific aspects, the thermodynamic parameters including band gaps, energies of defect formation and migration, are not the Eigenvalues of a Schrödinger equation describing the crystal. Such

parameters are defined statistically in terms of reactions occurring among ensembles of all possible configurations of the system.

The governing law of the equilibrium concentration of point defects introduced into a perfect semiconductor crystal is given for a neutral point defect X^0 by the expression [25]:

$$\frac{[X^0]}{[S]} = \theta_{X^0} \exp\left[\frac{-G^f_{X^0}}{kT}\right] \tag{II.2}$$

where [*S*] is the concentration of available lattice sites in the crystal, θ_{X^0} is the number of degrees of internal freedom of the defect on a lattice site, and $G^f_{X^0}$ is the standard Gibbs free energy. The parameters *k* and *T* respectively represent Boltzmann's constant and temperature.

In order to get an accurate model of the real defects equilibrium inside the bulk semiconductor, the enthalpy of formation need not refer only to elementary point defects such as interstitial, but also supports more complicated defect cluster formation encompassing a wide variety of defects including the divacancy, diinterstitial and vacancy-dopant pair, where we find in literature numerous methods for calculating the formation enthalpy of a defect pair and more progress still take place [26].

Characterization methods

In order to study defect properties, several experimental techniques have been used. Some of these approaches can be extended to deal with new materials and organic semiconductors. There is no universal approach suited to all situations, so continual improvement consists a major concern. However, two basic methods have been used abundantly in experimental applications [27], the first on is deep level transient spectroscopy (DLTS) developed by Lang in 1974, it exhibits its highest performances under ideal circumstances where it can reach defect concentrations as low as 10–6 times the carrier concentration of the semiconductor. By mean of this technique, it's also possible to identify radiation induced defects.

The key feature of DLTS consists in the limitation of emission rate so that only values of the capacitance transient within this range are extracted by the measurement apparatus. With the temperature variation, a peak in the instrument response is observed at the temperature associated with the trap emission rate. The sensitivity of DLTS when used in the capacitive mode decreases linearly with the distance towards the junction. Small uncertainties in the determination of the position of a DLTS peak can cause significant errors in the evaluation of the parameters of electronic states deep within the band gap; it is difficult to distinguish defects that are very close in energy.

Although DLTS is spectroscopic in nature giving trap energies, it has some undesirable properties: namely the large effort required in sample preparation and the limitation to samples of certain doping concentrations.

The second more versatile technique known as positron annihilation spectroscopy (PAS), is the spectroscopy of gamma (γ) rays emerging from the annihilation of positrons and electrons. The method is based on using the energy and momentum conservation during the annihilation process to study solids taking the advantage of parameters sensitivity to lattice imperfections (see Figure. II.3). When a positron is trapped in an open-volume defect, such as vacancies and dislocations, the annihilation parameters are modified in a characteristic way. Its lifetime increases due to the lower electron density. Momentum conservation leads to a small angular spread of the collinear γ –quanta or a Doppler shift of the annihilation energy [28]. Most positron lifetimes for the important semiconductors and lifetimes for various vacancy-type defects have been experimentally determined. Neutral and negative vacancy-type defects, as well as negative ions, are the dominant positron traps in semiconductors. Temperature-dependent lifetime measurements may distinguish between both defect types.

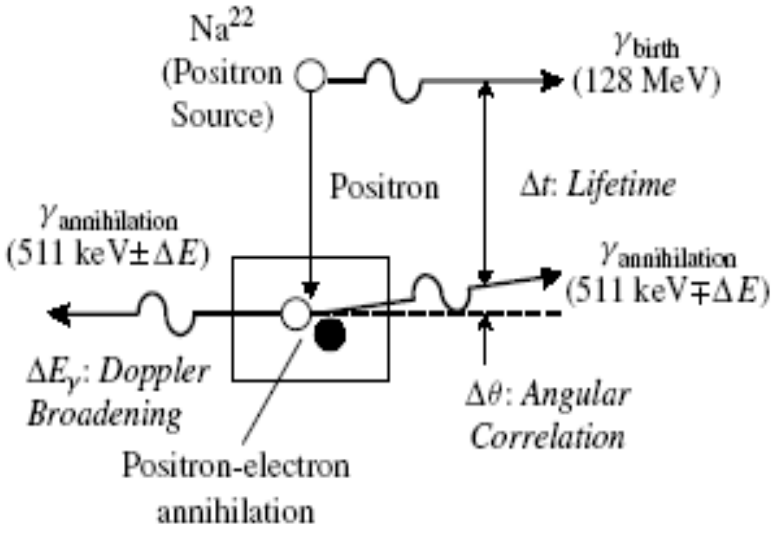


Fig. II.3. Schematic illustration of positron annihilation showing positron creation, positronelectron annihilation, γ emission and the main experimental techniques for PAS.

The intricate challenge facing the practical implementation of the method is the high costs of equipment not readily available to most researchers.

II.2.2. Hot carrier

In the last years, numerous studies have been revised and enhanced to get more adequate models regarding the hot carrier induced device degradation. In fact, the phenomenon has been observed or implemented under special forms in some types of Random Access Memory cells [29]. With the recent trends in nanodevices manufacturing, condensed efforts are invested to gain higher immunity performances without altering the optimal function of the device.

II.2.2.1. Origin of the problem

Under the bias conditions of a MOSFET structure, large electric fields are created along the device channel, as a result, carriers gain sufficiently high energies that allow their injection into the surrounding dielectric films such as the gate and sidewall oxides. The accumulation of mobile carriers at interfaces over long periods of operation can dramatically trigger many harmful physical processes causing the circuit in the worst case to fail. The hot carrier degradation process in a DG MOSFET device generates a second region having distinct properties influencing the behavior of the device as shown in figure II.4.

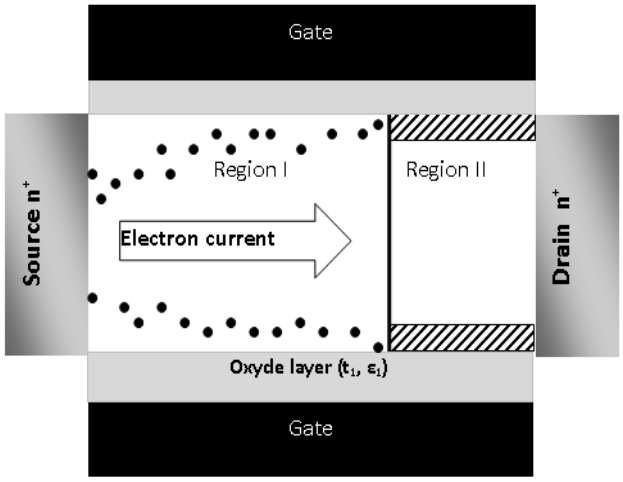


Fig. II.4. Creation of a damaged region in the DG MOSFET structure because of hot-carrier degradation process.

A more vigilant analysis indicates that the process takes initially place near the drain side where a drain substrate junction is created due to the formation of a pinch-off region. The lateral electric field exhibits a sharp peak in this region increasing with the shrink of channel length, as stated by figure II.5. The tunneling effect caused by the application of high drain biases, results in carriers penetration through the considered region and exhibition of non-equilibrium energy distributions. As a consequence, the concentration of energetic carriers

available for injection into the oxide requires the accurate calculation of electric field distribution in silicon because of the strict dependency between both quantities.

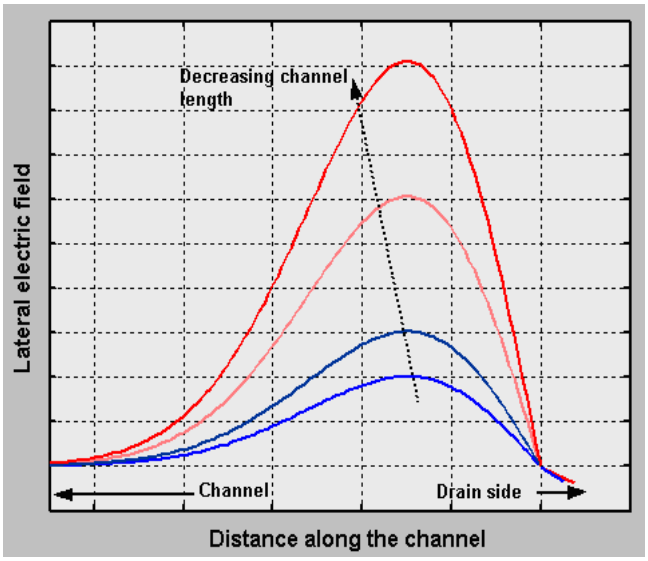


Fig. II.5. Maximum lateral electric field at the Si-SiO_2 interface along the channel in MOS transistors with decreasing channel lengths.

In both n and p-channel MOSFETs, vulnerabilities towards the injection of hot carriers have been detected, electrically active defects are generated in the oxide and at the Si-SiO_2 interface [30]. At advanced stages of the process, the energy gained by the carriers in the high field region of the silicon substrate induces the break of bonds associated with extrinsic or intrinsic defects in the oxide, and such rearrangement in its atomic structure is the generator factor of the device instabilities observed during the hot-carrier injection. The different mechanisms leading to MOSFET degradation are summarized on figure. II.6.

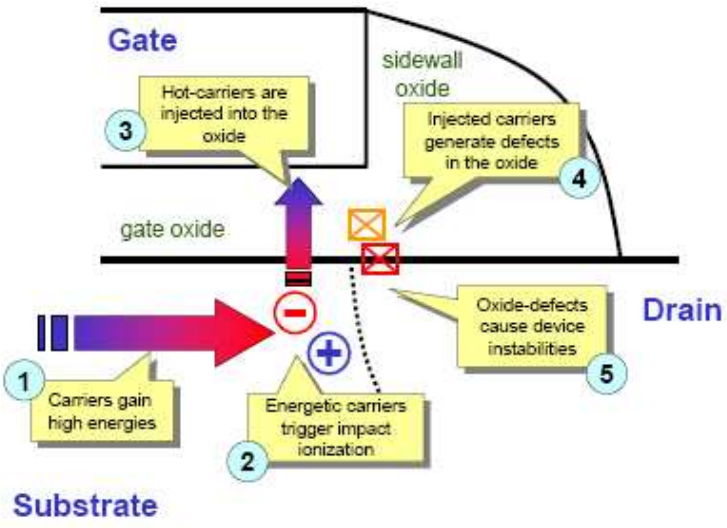


Fig. II.6. Sequence of physical mechanisms that contribute to HC-induced device degradation in MOS transistors.

II.2.2. 2. Device Parameter Shift

The presence of trapped charge and interface traps in the device due to HC injection directly affects the device operation. The amount of damage caused by hot-carriers is typically measured in terms of the shift in certain device-level parameters such as the threshold voltage, subthreshold slope, transconductance, and drain current obtained by performing device characterization measurements before and after HC injection. Similar techniques are also used to characterize the oxide damage resulting from other stress conditions such as high oxide fields, Fowler-Nordheim injection, and radiation exposure. However, the HC-induced device degradation differs from most of these stress conditions in the fact that the damage caused during HC injection is highly localized. On the other hand, damage caused by exposure to ionizing radiation, for example, occurs relatively uniformly throughout the oxide. The localized nature of damage caused by HC injection implies that the interpretation of shift in device parameters under such stress conditions is significantly different from cases when the damage is uniform. For example, a change in the subthreshold slope of the device is typically associated with a change in the density of interface traps if the damage is uniform. However, similar shifts in subthreshold slope can also be observed through a localized increase in trapped charge density in the oxide near the drain region. Even though advanced characterization techniques such as charge pumping measurements provide better understanding of the nature of HC induced device degradation, it is often essential to utilize device simulation tools along with the characterization experiments to gain better insight into the physical processes responsible for hot-carrier induced parameter shifts. In order to aid this process, device simulation tools must be able to model the influence of hot-carrier induced trapped charge and interface traps on the device characteristics.

The increase of interface trap charge density leads to an increase of the threshold voltage, it is observed that the variation of the threshold voltage with stressing time *t* follows a power law given by [31]:

$$\frac{\Delta V_{th}}{V_{th0}} = k_1 t^{n1} \tag{II.3}$$

It was also observed that another effect of the damage due to hot carriers consists in the drop of mobility of electrons in the inversion layer after stress. This is because with the increase of interface traps density with stress, the charge trapped at the interface traps also increases and affects the mobility of the channel carriers through Coulomb scattering. A drop in mobility and an increase of threshold voltage lead to a lower drain current in the device, the normalized

variation of drain current with stress time are similar to the threshold voltage, the normalized variation of the drain current with stress time follows a power law.

As a result of the drop in the biasing current of the transistor and the channel carrier mobility, the transconductance g_m also decreases. It is possible that the degradation of mobility due to stress is the dominant factor in the decrease of both the drain current and the transconductance, which also could be the reason why coefficients of the degradation laws are close, as the dominant degradation mechanism of both is the same. The slope of the I_{ds}–V_{ds} graphs in the saturation region is known as the output conductance g_{ds} of the transistor and gds can have an important effect on the operation of CMOS analog integrated circuits. From empirical results (Figure. II.7.), it was found that this slope changes with hot carrier stress. In contrast to threshold voltage and transconductance, the variations of g_{ds} with stress time when plotted in a log–log scale shows some saturation, especially at higher stress conditions [32].

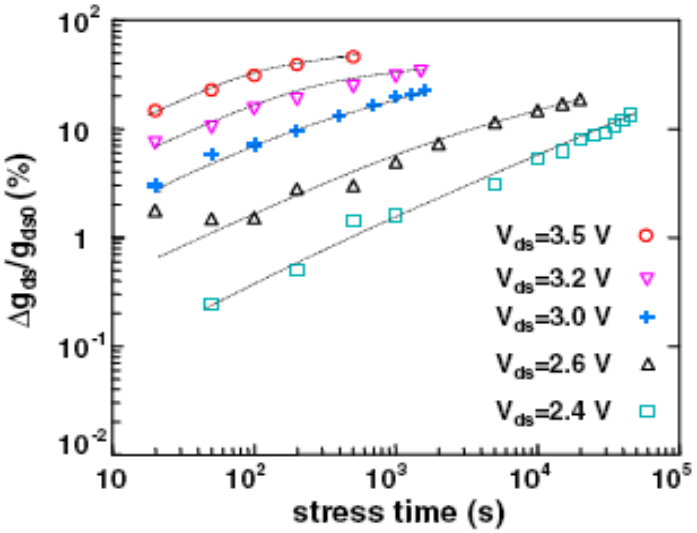


Fig. II.7. Normalized variation of the output conductance g_{ds} with stress time t.

In Table. II.1. a summary of important changes caused by hot-carrier stress is presented.

TABLE. II.1. Summary of important changes in the single NMOSFET

Parameter	**Direction of change**
Threshold voltage V_{th}	Increases
Drain current I_{ds}	Decreases
Transconductance g_m	Decreases
Output conductance g_{ds}	Increases

II.3. DEVICE DEGRADATION MODELS

In order to predict the device degradation due to hot-carrier injection under circuit operation, several empirical and semi-empirical models have been suggested in the past literature. This section provides an overview of some of the most popular models that are presently being used to model parameter shifts and device lifetimes.

- *Takeda and Suzuki Model*

Takeda and Suzuki [33] suggested a simple time dependent model for parameter shifts based on the experiments performed under the $I_{B;max}$ condition. In their experiments, they observed that ΔV_T or $\%\Delta Gm$ could be modeled empirically using expressions such as:

$$\%\Delta G_m = At^n \tag{II.4}$$

where, A and n are empirical parameters extracted separately for each technology. The parameter n has a strong dependence on the gate bias used during the stressing experiments but little dependence on the drain bias. Similarly, the parameter A shows a strong dependence on the drain bias while its independent of the gate bias. In order to allow extrapolation from the drain bias used under stressing conditions to real-life drain biases, the dependence of A on the drain bias can be modeled as:

$$A\alpha \exp\left(-\frac{1}{V_{DS}}\right) \tag{II.5}$$

The simplicity of this model allows quick and easy extrapolation of device lifetimes under stressing conditions to the real-life biases. This approach has been used extensively for fast first-order benchmarking of different technologies. In the past, a duty-cycle based extension of this model has been applied to evaluate device lifetime under AC operation [34]. However, this model finds little application in predicting the dynamic degradation of present generation MOSFETs.

- *Hu Model*

Hu et al.[35] extended the lucky electron approach to obtain a semi-empirical model for predicting device degradation under circuit operation. The physical basis of this model and the use of this model in circuit reliability simulators such as BERT has made this the most popular hot-carrier degradation model for n-channel MOSFETs. A complete analysis and the assumptions involved in this model can be found elsewhere. For the purpose of this work, we will use a popular form of this model as given by:

$$\%\Delta G_m(t) = \left[A\int_0^t \left[\frac{I_B}{I_{DS}}\right]^m I_{DS}\,dt \right]^n \tag{II.6}$$

where, A, m, and n are empirical parameters. As the degradation model is driven by substrate and drain currents, it can be directly applied to device degradation under dynamic operation once the empirical parameters have been obtained from single-bias DC stressing experiments. This model assumes that the device degradation is entirely due to increase in the interface trap density and is usually parameterized using stressing experiments performed under the $I_{B;max}$ condition.

- *Woltjer Model*

The lucky-electron model predicts the interface trap generation at maximum-substrate current conditions but fails at other bias conditions. The model suggested by Woltjer et al.[36] incorporated the dependence on the oxide electric field in this model to extend it to all biases under which the effect of interface traps dominates. The influence of oxide charge has been avoided in this work by defining the device lifetime at a large number of interface states in terms of the change in charge pumping current. The effect of the charge has, however, been observed if the lifetime is defined as a smaller value. As interface trap generation depends approximately exponentially on the oxide electric field, $E_{ox} = (V_g\text{-}V_d\text{-}V_t)/t_{ox}$, the following correction to the "lucky-electron" model has been suggested:

$$\tau_{Icp} \alpha e^{E_{ox}/E_0} \tag{II.7}$$

where, τ_{Icp} is the charge-pump lifetime defined as $\tau_{Icp}/W/f = 100pA/m/Hz$ and E_o is an empirical parameter. The degradation data obtained on MOSFETs with different dimensions and oxide-thicknesses has been fitted to the following model using the same set of fitting parameters for the technology used:

$$\log_{10}(\tau_{Icp}) = \left[-A\log_{10}\left(\frac{I_b}{I_d}\right)\right]^n - \log_{10}\left(\frac{I_d}{W}\right) - \frac{E_{ox}}{E_0} + C_{W3} \tag{II.8}$$

where, A, n, E_o and C_{W3} are the fitting parameters. This gives the following relationship for the degradation of the charge-pumping current as a function of time:

$$\Delta I_{cp} = \left[\frac{C_4 \left[\frac{tI_d}{W}\left(\frac{1}{C_1}\right)^A \right]^n 10^{\frac{nE_{ox}}{E_0}}}{10^n \left[-A\log_{10}\left(\frac{I_d}{I_b}\right)\right]^n} \right] \tag{II.9}$$

- *Mistry et al. Approach*

In some of the recent studies involving dynamic stressing experiments, it was observed that degradation models based on a single degradation mechanisms failed to accurately predict the

degradation under dynamic operation. Mistry et al.[37] attributed this discrepancy to the presence of two different degradation modes during dynamic operation. As mentioned earlier, these three degradation modes correspond to stressing experiments performed under three different bias conditions: H_{inj}, $I_{B;max}$ and E_{inj}. Mistry et al. modeled the device lifetime under each of these bias conditions using three different models:

$$I_{B,\max} \qquad \tau_{I_{B,\max}} = AI_B^{-m} \tag{II.10.a}$$

$$H_{inj} \qquad \tau_{H_{inj}} = B\frac{\left(\frac{I_B}{I_{DS}}\right)^{-n}}{I_{DS}} \tag{II.10.b}$$

$$E_{inj} \qquad \tau_{E_{inj}} = C\frac{\left(\frac{I_G}{I_{DS}}\right)^{-l}}{I_{DS}} \tag{II.10.c}$$

The device lifetime under dynamic operation can be obtained in terms of these models using the following approach. If the terminal currents of the device are known as a function of time during the dynamic operation of the device, the contributions of each of the three degradation mechanisms over one cycle of the AC waveform can be calculated by integrating the individual models listed above:

$$\frac{1}{\tau_{I_{B,\max}}} = \frac{1}{AT}\int_0^T I_B^m dt \tag{II.11.a}$$

$$\frac{1}{\tau_{H_{inj}}} = \frac{1}{BT}\int_0^T \left(\frac{I_B}{I_{DS}}\right)^n I_{DS} dt \tag{II.11.b}$$

$$\frac{1}{\tau_{E_{inj}}} = \frac{1}{CT}\int_0^T \left(\frac{I_G}{I_{DS}}\right)^l I_{DS} dt \tag{II.11.c}$$

If each of the integral above can be treated as damage functions, the dynamic lifetime, τ_{AC}, can be obtained using a Matthiessen-like rule as follows:

$$\frac{1}{\tau_{AC}} = \frac{1}{\tau_{I_{B,\max}}} + \frac{1}{\tau_{H_{injx}}} + \frac{1}{\tau_{E_{inj}}} \tag{II.12}$$

This approach has been successfully applied to predict the device degradation under dynamic operation in simple digital CMOS circuits based on the three sets of single-bias DC stressing experiments. However, in order to be used in a circuit reliability simulator, a model for device degradation should predict the time dependence of the degradation rather than the lifetime. As the dynamic degradation of n-channel MOSFETs has been shown to have a much stronger

time dependence as compared to static degradation, the definition of the lifetime itself can affect the validity of lifetime models for certain technologies. Conventional models deviate from the observed values while the coupled application of three models results in an improved prediction as shown in figure. II.7.

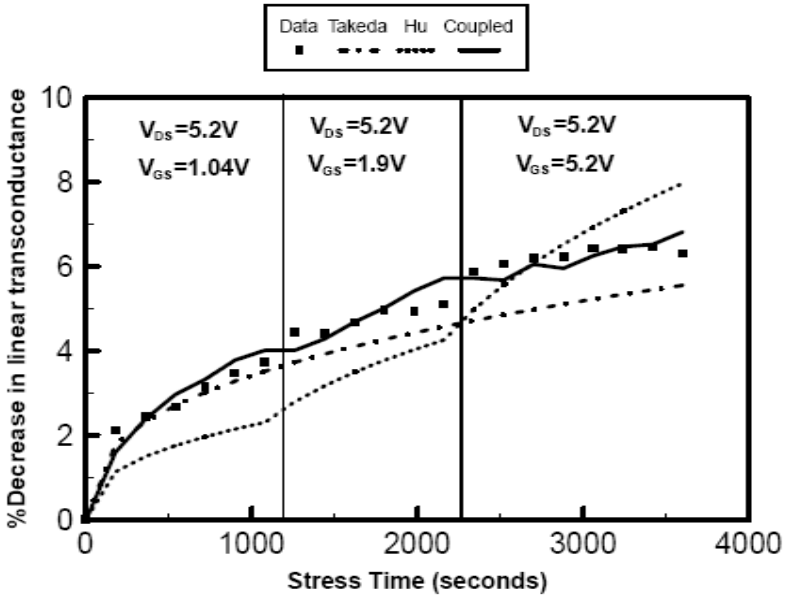


Fig. II.8. Device degradation for stressing under bias sequence [19].

II.4. CONCLUSION

In this chapter, we discussed the qualitative nature of the basic physical mechanisms responsible for hot-carrier-induced degradation in MOSFETs. The physical mechanisms described here represent effects that are active during the normal operation of such devices and result in shifts in experimentally measurable device parameters such as threshold voltage and linear transconductance. In order to aid this process, device simulation tools must be able to model the influence of hot-carrier induced trapped charge and interface traps on the device characteristics.

Chapter III –

MODELING OF GCGS DG MOSFET IN SUBTHRESHOLD REGION

Abstract: In order to pursue the miniaturization process as predicted by Moor's law and go beyond actual reached lengths, more condensed efforts should be focused not only on looking for higher mobility materials but also on improving existing topologies of nanocircuits digital devices, which are the bone stone of currently used information storage supports..

The aim of this chapter is to provide a quantitative proof about the efficiency of our proposed structure Graded Channel Gate Stack Double Gate MOSFET (GCGS DG MOSFET) in remedying the many degradation aspects caused by short channel and hot carriers effects. Our proposed structure shows reduced significantly the response to such altered behavior. Consequently, it can be reasonably claimed that the GCGS DG MOSFET structure can bring promised solutions for overcoming the downscaling imposed burdens.

III.1. INTRODUCTION

In recent years, design and fabrication of nanoscale MOSFETs have been received great interests for their high potential adaptability in advanced integration circuits design particularly CMOS based devices, an aggressive race was conducted by researchers to tackle the new challenges occurring due to the downscaling process [38]. In fact, the improvement of the MOSFET structure is a battle against the parasitic phenomena becoming clearer when the channel length shrinks down to nanoscale level. Among the main problems appearing because of miniaturization we find the short channel effects (SCE) and the hot carrier degradation effects, these undesirable phenomena are basically caused by the influence of the drain potential on the gate control over the channel, in addition to the presence of an interfacial charge density near the drain side. Consequently, the most obvious result of such situation is that various characteristics parameters are affected and became dependent on channel length.

Due to the high costs required for practical implementation of nano-devices, the need for other performance criteria measure approaches that are easier to develop is vital [39], numerical simulation can be considered as a paramount solution for the design and optimization of novel semiconductor devices. Hence, the suitability of simulation to this field is an undiscussed reality.

The main goal of this chapter is to investigate the appropriateness of our proposed Graded Channel Gate Stack Double Gate MOSFET (GCGS DG MOSFET) structure in dealing essentially with the hot-carrier degradation effects. Motivated by the many lacks of conventional MOSFET in nanoscale regime, we examine the possibility of developing new models assessing the performances of our structure under different combined constraints. Our approach for developing such models is based on the surface-potential formalism, which will not only enable the accurate description of the GCGS DG MOSFET behavior, but will also facilitate the incorporation of new added conditions to the whole approach when needed. The rest of this chapter is partitioned as follows: Section III.2. provides the modeling approach for principal parameters. Section III.3. presents and discuss simulation results. Finally, Section III.4. summarizes some concluding notes.

III.2. MODEL FORMULATION

III.2.1. Surface potential

A detailed view of the nanoscale GCGS DG MOSFET is depicted in figure.III.1. By definition, the whole channel is constituted of a low doping concentration (N_{AL}) region and a high doping concentration (N_{AH}) one [40], if we assume the existence of an interfacial charge density (N_f) near the drain [41], thus the high doping concentration region can be divided into fresh and damaged subregions. The total length of the channel is L, the lengths of the fresh subregions I and II are denoted by L_1 and L_2 respectively, whereas the length of the damaged subregion can be deduced as $L_d = L - L_1 - L_2$. The structure is symmetric with a double-layer gate stack, oxide and high-k layers, the doping level of the drain/source region is given by $N_{D/S}$ respectively.

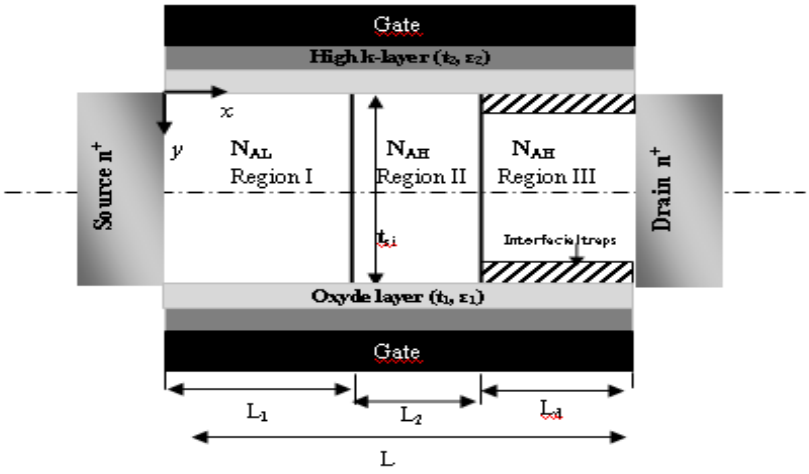


Fig. III.1. Cross-sectional view of the GC GS DG MOSFET proposed inner structure.

Since the electrostatics potential inside the channel is described by the 2-D Poisson partial differential equation:

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{qN_A}{\varepsilon_{Si}} \tag{III.1}$$

subject to the boundary conditions:

$$\varepsilon_{ox}\frac{V_{F,eff}-\psi(x,0)}{t_{oxeff}}=\varepsilon_{Si}\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y=0} \tag{III.2.a}$$

$$\varepsilon_{ox}\frac{V_{B,eff}-\psi(x,t_{Si})}{t_{oxeff}}=\varepsilon_{Si}\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y=t_{si}} \tag{III.2.b}$$

$$\psi(0,y) = V_{bi} \tag{III.2.c}$$

$$\psi(L,y) = V_{bi} + V_{ds} \tag{III.2.d}$$

so we have to resolve such boundary problem separately for each subregion after adding two new conditions defined on intermediate frontiers:

$$\psi(L_1,y) = V_{p1} \tag{III.3.a}$$

$$\psi(L_1 + L_2,y) = V_{p2} \tag{III.3.b}$$

where ε_{ox} is the oxide permittivity, t_{si} is the thickness of silicon channel. V_{bi} is the junction voltage between the source/drain and intrinsic silicon with $V_{bi} = (kT/q)\ln(N_{D/S}/n_i)$, n_i is the intrinsic silicon density and V_{ds} is the drain to source voltage.

The introduction of effective voltages at the front and bottom gates allow to alleviate derivations for symmetric structure as follows:

$$V_g^* = V_{F,eff} = V_{B,eff} = V_{gs} - \phi_{MS} \tag{III.4}$$

where ϕ_{MS} is the gate work function referenced to intrinsic silicon and V_{gs} represents the gate source voltage. The effective oxide layer thickness of insulator layer t_{oxeff} is given by the superposition of the thickness of the SiO_2 layer t_1 ($\varepsilon_{ox} = \varepsilon_1$) and the thickness of the high-k layer t_2 (ε_2) as follows:

$$t_{oxeff} = t_1 + (\varepsilon_1/\varepsilon_2)t_2 \tag{III.5}$$

Young's pioneer work showed that by taking a particular profile for the potential distribution, many simplifications are provided in term of computational complexity [42]. By adopting the same scheme expressed by a parabolic profile as:

$$\psi(x,y) = a(x) + b(x)y + c(x)y^2 \tag{III.6}$$

we can transform our initial boundary problem to an ordinary differential equation that is much easier to resolve.

After application of the boundary conditions and $\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y=t_{Si}/2} = 0$ known as the symmetry condition, yields the formula describing the channel potential distribution:

$$\psi(x,y) = \psi_s(x) + \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\psi_s(x) - V_g^*}{t_{oxeff}}y - \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\psi_s(x) - V_g^*}{t_{oxeff}t_{Si}}y^2 \tag{III.7}$$

where $\Psi_s(x)$ represents the surface potential at Si/SiO_2 frontiers given by $y=0$ and $y=t_{si}$.

Substituting (III.7) in (III.1), an ordinary differential equation dealing only with the surface potential is obtained:

$$\frac{d^2\psi_s(x)}{dx^2} - \frac{1}{\lambda^2}\psi_s(x) = D \tag{III.8}$$

The general solution of such equation is the sum of the complementary solution given by $A_1 e^{\frac{x}{\lambda}} + A_2 e^{-\frac{x}{\lambda}}$ associated with the homogeneous equation and the particular solution easily guessed to be $-\lambda^2 D$. Thus, the general solution of (III.8) has the form $\psi_s(x) = -\lambda^2 D + A_1 e^{\frac{x}{\lambda}} + A_2 e^{-\frac{x}{\lambda}}$, where A_1 and A_2 are constants determined by satisfying the boundary conditions [43].

In region I ($0 \le x \le L_1$) the equation to be solved is:

$$\frac{d^2\psi_{s1}(x)}{dx^2} - \frac{1}{\lambda^2}\psi_{s1}(x) = D_1 \tag{III.9}$$

with $\lambda = \frac{\varepsilon_{si} \cdot t_{oxeff} \cdot t_{si}}{2\varepsilon_1}$ and $D_1 = \frac{qN_{AL}}{\varepsilon_{si}} - \frac{1}{\lambda^2}V_g^*$

under the following boundary conditions:

$$\psi(0, y) = V_{bi}$$

$$\psi(L_1, y) = V_{p1}$$

After some mathematical manipulations we deduce:

$$\psi_{s1}(x) = -\lambda^2 D_1 + \frac{\phi_{D1}\sinh\left(\frac{x}{\lambda}\right) - \phi_{s1}\sinh\left(\frac{x - L_1}{\lambda}\right)}{\sinh\left(\frac{L_1}{\lambda}\right)} \tag{III.10}$$

with $\phi_{D1} = V_{p1} + \lambda^2 D_1$ and $\phi_{s1} = V_{bi} + \lambda^2 D_1$

In region II ($L_1 \le x \le L_1 + L_2$), by following the same methodology as above for the following problem:

$$\frac{d^2\psi_{s2}(x)}{dx^2} - \frac{1}{\lambda^2}\psi_{s2}(x) = D_2 \tag{III.11}$$

$$\text{with } D_2 = \frac{qN_{AH}}{\varepsilon_{si}} - \frac{1}{\lambda^2}V_g^*$$

under the following boundary conditions:

$\psi(L_1, y) = V_{p1}$

$\psi(L_1 + L_2, y) = V_{p2}$

The obtained solution is:

$$\psi_{s2}(x) = -\lambda^2 D_2 + \frac{\phi_{s2}\sinh\left(\frac{x-L_1}{\lambda}\right) - \phi_{D2}\sinh\left(\frac{x-L_1-L_2}{\lambda}\right)}{\sinh\left(\frac{L_2}{\lambda}\right)} \quad \text{(III.12)}$$

with $\phi_{s2} = V_{p2} + \lambda^2 D_2$ and $\phi_{D2} = V_{p1} + \lambda^2 D_2$

In region III ($L_1 + L_2 \le x \le L$), by the same manner for the equation:

$$\frac{d^2\psi_{s3}(x)}{dx^2} - \frac{1}{\lambda^2}\psi_{s3}(x) = D_3 \quad \text{(III.13)}$$

with $D_3 = \frac{qN_{AH}}{\varepsilon_{si}} - \frac{1}{\lambda^2}V_g^* - \frac{qN_f}{C_{ox}}$ and C_{ox} is the oxide capacitance [44].

under the following boundary conditions:

$\psi(L_1 + L_2, y) = V_{p2}$

$\psi(L, y) = V_{bi} + V_{ds}$

Some mathematical simplifications lead to the solution:

$$\psi_{s3}(x) = -\lambda^2 D_3 + \frac{\phi_{D3}\sinh\left(\frac{x-L_1-L_2}{\lambda}\right) - \phi_{s3}\sinh\left(\frac{x-L}{\lambda}\right)}{\sinh\left(\frac{L-L_1-L_2}{\lambda}\right)} \quad \text{(III.14)}$$

with $\phi_{D3} = V_{bi} + V_{ds} + \lambda^2 D_3$ and $\phi_{s3} = V_{p2} + \lambda^2 D_3$

V_{p1} and V_{p2} which denote potentials at the boundaries can be deduced by resolving the linear system given below, which reflects the continuity equation of the electric field at $x=L_1$ and at $x=L_1+L_2$:

$$\begin{cases} \left.\frac{\partial\psi_{s1}(x)}{\partial x}\right|_{x=L_1} = \left.\frac{\partial\psi_{s2}(x)}{\partial x}\right|_{x=L_1} \\ \left.\frac{\partial\psi_{s2}(x)}{\partial x}\right|_{x=L_1+L_2} = \left.\frac{\partial\psi_{s3}(x)}{\partial x}\right|_{x=L_1+L_2} \end{cases} \quad \text{(III.15)}$$

Using the well-known determinant method we get at the end the following expressions:

$$\begin{cases} V_{p1} = \frac{\alpha_1 D_1 + \beta_1 D_2 + \gamma_1 D_3 + \delta_1}{\chi_1} \\ V_{p2} = \frac{\alpha_2 D_1 + \beta_2 D_2 + \gamma_2 D_3 + \delta_2}{\chi_2} \end{cases} \quad \text{(III.16)}$$

where α_i, β_i, γ_i, δ_i and χ_i ; *i=1,2* are known factors depending on parameters *L*, L_1, L_2 , V_{bi}, V_{ds} and λ.

III.2.2.Threshold voltage

Based on the set of expressions defining the surface potential in each subregion, the threshold voltage can be calculated using the famous condition of the minimum channel potential:

$$\psi_s(x_{\min})\big|_{V_{gs}=V_{th}} = 2\phi_B \tag{III.17}$$

where ϕ_B represents the bulk potential of silicon body given as $\phi_B = (kT/q)\ln(N_{AL/AH}/n_i)$.

The location of the minimum surface potential along the channel is obtained by solving the basic equation for all subregions:

$$\frac{\partial \psi_{s1,s2,s3}(x)}{\partial x} = 0 \tag{III.18}$$

Without big difficulty, we get the following results:

$$x_{\min 1} = \frac{1}{2}\left[L_1 - \lambda \ln\left(\frac{\phi_{s1} - \phi_{D1}e^{\frac{L_1}{\lambda}}}{\phi_{D1} - \phi_{s1}e^{\frac{L_1}{\lambda}}}\right)\right] \tag{III.19.a}$$

$$\psi_{s1\min} = -\lambda^2 D_1 + \frac{\phi_{D1}\sinh\left(\frac{x_{\min 1}}{\lambda}\right) - \phi_{s1}\sinh\left(\frac{x_{\min 1} - L_1}{\lambda}\right)}{\sinh\left(\frac{L_1}{\lambda}\right)} \tag{III.19.b}$$

$$x_{\min 2} = \frac{1}{2}\left[2L_1 + L_2 + \lambda \ln\left(\frac{\phi_{D2}e^{\frac{L_1+L_2}{\lambda}} - \phi_{s2}e^{\frac{L_1}{\lambda}}}{\phi_{s2}e^{\frac{L_1+L_2}{\lambda}} - \phi_{D2}e^{\frac{L_1}{\lambda}}}\right)\right] \tag{III.19.c}$$

$$\psi_{s2\min} = -\lambda^2 D_2 + \frac{\phi_{s2}\sinh\left(\frac{x_{\min 2} - L_1}{\lambda}\right) - \phi_{D2}\sinh\left(\frac{x_{\min 2} - L_1 - L_2}{\lambda}\right)}{\sinh\left(\frac{L_2}{\lambda}\right)} \tag{III.19.d}$$

$$x_{\min 3} = \frac{1}{2}\left[L + L_1 + L_2 + \lambda \ln\left(\frac{\phi_{s3}e^{\frac{L}{\lambda}} - \phi_{D3}e^{\frac{L_1+L_2}{\lambda}}}{\phi_{D3}e^{\frac{L}{\lambda}} - \phi_{s3}e^{\frac{L_1+L_2}{\lambda}}}\right)\right] \tag{III.19.e}$$

$$\psi_{s3\min} = -\lambda^2 D_3 + \frac{\phi_{D3}\sinh\left(\frac{x_{\min 3} - L_1 - L_2}{\lambda}\right) - \phi_{s3}\sinh\left(\frac{x_{\min 3} - L}{\lambda}\right)}{\sinh\left(\frac{L - L_1 - L_2}{\lambda}\right)} \quad \text{(III.19.f)}$$

It should be pointed out that the minimum surface potential is specified in a global manner by taking:

$$\psi_{s\min} = \min\left(\psi_{s1\min}, \psi_{s2\min}, \psi_{s3\min}\right) \quad \text{(III.20)}$$

If we assume that the minimum surface potential is located in the first healthy subregion, then, we have to manipulate the equation:

$$\psi_{s\min} = \psi_{s1\min} = -\lambda^2 D_1 + \frac{\phi_{D1}\sinh\left(\frac{x_{\min 1}}{\lambda}\right) - \phi_{s1}\sinh\left(\frac{x_{\min 1} - L_1}{\lambda}\right)}{\sinh\left(\frac{L_1}{\lambda}\right)} = 2\phi_B \quad \text{(III.21)}$$

Finally, some mathematical simplifications lead us to the formula [45]:

$$\sqrt{\left(-\phi_{D1}^2 - \phi_{s1}^2 + 2\phi_{D1}\phi_{s1}\cosh\left(\frac{L_1}{\lambda}\right)\right)} + \left(\lambda^2 D_1 + 2\phi_B\right)\sinh\left(\frac{L_1}{\lambda}\right) = 0 \quad \text{(III.22)}$$

It should be noted that such equation can be easily transformed to an equivalent second degree algebraic one dealing with the threshold voltage explicitly. So, the application of the familiar quadratic formula suffices to get the threshold voltage. Despite that two possible solutions are valid theoretically; the wrong one meaningless physically is eliminated by taking into consideration the fact that the device is high sensitive in addition to the good correspondence with the fresh device when hot-carriers effects are neglected.

III.2.3. Subthreshold current

To study the subthreshold current in presence of the hot-carriers degradation effects, we should first determine the properties and characteristics of the current density. It's important to mention that despite its composition of both terms of drift and diffusion currents and due to the weak inversion region, the diffusion one dominates. In this case, the current is proportional to the electron concentration at the virtual cathode. By adopting in a similar way the methodology proposed for 4-T and 3-T DG MOSFET [46], an explicit analytical subthreshold current equation is derived for our GCGS DG MOSFET as follows:

$$J_n(y) = qD_n \frac{n_{\min}(y)}{L}\left(1 - e^{\frac{V_{ds}}{V_t}}\right) \tag{III.23}$$

where D_n denotes the diffusion constant and V_t is the thermal voltage. The potential is minimum at a fixed location along the channel where the carriers concentration is given by $n_{min}(y)$. Such quantity can be calculated by substituting the minimum potential into Boltzmann distribution and the electrons density at virtual cathode can be defined as:

$$n_{\min}(y) = \left(\frac{n_i^2}{N_{CH}}\right) e^{\frac{\psi_{\min}(y)}{V_t}} \tag{III.24}$$

The subthreshold current adapted to our GCGS DG MOSFET model including interfacial traps effects is obtained by integrating (III.23) along the silicon film to get:

$$I_{sub} = I_{sub1} + I_{sub2} + I_{sub3} \tag{III.25}$$

with I_{sub1}, I_{sub2} and I_{sub3} are the subthreshold currents associated with the first, second and third subregions respectively which are defined by:

$$I_{sub1} = \frac{2k_1V_t}{E_s}\left(e^{\frac{\psi_{\min}}{V_t}} - e^{\frac{\psi^s_{\min}}{V_t}}\right) \tag{III.26.a}$$

$$I_{sub2} = \frac{2k_2V_t}{E_s}\left(e^{\frac{\psi_{\min}}{V_t}} - e^{\frac{\psi^s_{\min}}{V_t}}\right) \tag{III.26.b}$$

$$I_{sub3} = \frac{2k_3V_t}{E_s}\left(e^{\frac{\psi^s_{\min}}{V_t}} - e^{\frac{\psi_{\min}}{V_t}}\right) \tag{III.26.c}$$

with

$$k_1 = \left(\frac{q\mu_n WV_t n_i^2}{L_1 N_{AL}}\right) \times \left(1 - e^{-\frac{V_{p1}}{V_t}}\right)$$

$$k_2 = \left(\frac{q\mu_n WV_t n_i^2}{L_2 N_{AH}}\right) \times \left(1 - e^{-\frac{V_{p1}}{V_t}}\right)$$

$$k_3 = \left(\frac{q\mu_n WV_t n_i^2}{(L - L_1 - L_2) N_{AH}}\right) \times \left(1 - e^{-\frac{(V_{ds} - V_{p2})}{V_t}}\right)$$

$$E_s = 2(\psi_{\min} - \psi^s_{\min})/t_{si}$$

$$\psi^s_{\min} = \psi(x_{\min}, 0)$$

$$\psi_{\min} = \psi(x_{\min}, t_{si}/2)$$

If the damaged subregion is extended to the whole high doping concentration region ($L_2 \to 0$), our initial analytical subthreshold current model reduces to following simple expression:

$$I_{sub} = I_{sub1} + I_{sub2} \tag{III.27}$$

with I_{sub1}, and I_{sub2} are the subthreshold currents associated with the low doping concentration subregion and the high doping concentration completely damaged subregion:

$$I_{sub1} = \frac{2k_1 V_t}{E_s}\left(e^{\frac{\psi_{\min}}{V_t}} - e^{\frac{\psi^s_{\min}}{V_t}} \right) \tag{III.28.a}$$

$$I_{sub2} = \frac{2k_2 V_t}{E_s}\left(e^{\frac{\psi^s_{\min}}{V_t}} - e^{\frac{\psi_{\min}}{V_t}} \right) \tag{III.28.b}$$

with

$$k_1 = \left(\frac{q\mu_n W V_t n_i^2}{L_1 N_{AL}} \right) \times \left(1 - e^{-\frac{V_p}{V_t}} \right)$$

$$k_2 = \left(\frac{q\mu_n W V_t n_i^2}{L_2 N_{AH}} \right) \times \left(1 - e^{-\frac{(V_{ds} - V_p)}{V_t}} \right)$$

$$E_s = 2\left(\psi_{\min} - \psi^s_{\min}\right)/t_{si}$$

$$\psi^s_{\min} = \psi\left(x_{\min}, 0\right)$$

$$\psi_{\min} = \psi\left(x_{\min}, t_{si}/2\right)$$

where V_p is the potential at the boundary given by:

$$V_p = \frac{\phi_{s2}\sinh\left(\frac{L_1}{\lambda}\right) + \phi_{s1}\sinh\left(\frac{L - L_1}{\lambda}\right) - \alpha\lambda^2 D_2 + \beta\lambda^2 D_1}{\sinh\left(\frac{L}{\lambda}\right)}$$

with $\alpha = \sinh\left(\frac{L_1}{\lambda}\right)\cosh\left(\frac{L - L_1}{\lambda}\right)$ and $\beta = \cosh\left(\frac{L}{\lambda}\right)\sinh\left(\frac{L - L_1}{\lambda}\right)$

III.2.4. Subthreshold swing

Based on the previous assumption about proportionality between the drain current and the free carriers density at the virtual cathode following the Boltzmann distribution function, the general subthreshold swing (S) model is given by:

$$S = \frac{\partial V_{gs}}{\partial \log I_{ds}} = V_t \ln(10) \times \left[\frac{\int_0^{t_{si}/2} e^{\psi_{\min}/V_t}\left(\frac{\partial \psi_{\min}}{\partial V_{gs}}\right) dy}{\int_0^{t_{si}/2} e^{\psi_{\min}/V_t} dy} \right]^{-1} \tag{III.29}$$

An approximate solution for this integral was proved to have the form:

$$S = \frac{kT}{q}\ln(10)\times\left[\frac{\partial \psi_{s\min}}{\partial V_{gs}}\right]^{-1} \tag{III.30}$$

Hence, a closed form expression for subthreshold swing for our GCGS DG MOSFET with the hot-carriers degradation effects can be written in case of $0 \le x_{\min} \le L_1$ as:

$$S = \frac{kT}{q}\ln(10)\times[1+\xi]^{-1} \tag{III.31}$$

with

$$\xi = \frac{a + b\left(\dfrac{\sinh\left(\frac{L-L_1}{\lambda}\right)+\sinh\left(\frac{L_1}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\right)}{2\sinh\left(\frac{L1}{\lambda}\right)\times\left[-\phi_{s1}^2-\phi_{D1}^2+2\phi_{s1}\phi_{D1}\cosh\left(\frac{L_1}{\lambda}\right)\right]^{\frac{1}{2}}}$$

where $\begin{cases} a = 2\phi_{s1} - 2\phi_{D1}\cosh\left(\frac{L_1}{\lambda}\right) \\ b = 2\phi_{D1} - 2\phi_{s1}\cosh\left(\frac{L_1}{\lambda}\right) \end{cases}$

A more elementary model can be deduced with some approximations and simplifications as:

$$S = \frac{kT}{q}\ln(10)\left[1+\frac{\sinh\left(\frac{x_{\min1}-L_1}{\lambda}\right)-\sinh\left(\frac{x_{\min1}}{\lambda}\right)-\sigma}{\sinh\left(\frac{L_1}{\lambda}\right)}\right]^{-1} \tag{III.32}$$

with

$$\sigma = \frac{(a_1+a_2+a_3)\sinh\left(\frac{x_{\min1}}{\lambda}\right)}{\sinh\left(\frac{L_1+L_2}{\lambda}\right)\sinh\left(\frac{L-L_1}{\lambda}\right)-\sinh\left(\frac{L_1}{\lambda}\right)\sinh\left(\frac{L-L_1-L_2}{\lambda}\right)}$$

$$a_1 = \sinh\left(\frac{L_2}{\lambda}\right)\sinh\left(\frac{L-L_1}{\lambda}\right)\times\left(1-\cos\left(\frac{L_1}{\lambda}\right)\right)$$

$$a_2 = \sinh\left(\frac{L_1}{\lambda}\right)\times\left(1-\cosh\left(\frac{L_2}{\lambda}\right)\right)\times\left(\sinh\left(\frac{L-L_1}{\lambda}\right)+\sinh\left(\frac{L-L_1-L_2}{\lambda}\right)\right)$$

$$a_3 = \sinh\left(\frac{L_2}{\lambda}\right)\times\sinh\left(\frac{L_1}{\lambda}\right)\times\left(1-\cosh\left(\frac{L-L_1-L_2}{\lambda}\right)\right)$$

For a high doping concentration completely damaged region $L_2 \to 0$. Therefore, a new closed form relation is obtained as:

$$S = \frac{kT}{q}\ln(10)\times\left[1+\frac{-\left(\sinh\left(\frac{L_1}{\lambda}\right)+\sinh\left(\frac{L-L_1}{\lambda}\right)\right)\gamma+\sinh\left(\frac{x_{min1}-L_1}{\lambda}\right)}{\sinh\left(\frac{L_1}{\lambda}\right)}\right]^{-1} \quad \text{(III.33)}$$

with $\gamma = \dfrac{\sinh\left(\frac{x_{\min 1}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$

For long channel device ($L >> \lambda$), a simple new analytical subthreshold swing model can be expressed as:

$$S = \frac{kT}{q}\ln(10)\times\left[1+\frac{\sinh\left(\frac{x_{\min 1}-L_1}{\lambda}\right)}{\sinh\left(\frac{L_1}{\lambda}\right)}\right]^{-1} \quad \text{(III.34)}$$

III.3. RESULTS AND DISCUSSION

Parameter values used for the simulation are summarized in TABLE .III.3.

TABLE .III.3. Values of parameters used in the analysis.

Parameter	**Value**
L	2×10^{-6} cm
W	1×10^{-6} cm
t_{si}	1×10^{-6} cm
t_1	1×10^{-7} cm
t_2	1.5×10^{-7} cm
ε_1	3.9
ε_2	10
n_i	1.45×10^{10} cm^{-3}
N_{AL}	1×10^{15} cm^{-3}
N_{AH}	1×10^{17} cm^{-3}
μ	1400 $cm^2/V.s$
ND	1×10^{20} cm^{-3}
NS	1×10^{20} cm^{-3}

Figure.II.2. shows the variation of surface potential along the channel for GCGS and conventional DG MOSFETs for L=20 nm. Two interesting features can be easily observed, first, the incorporation of GCGS design introduces a shift in the surface potential profile along the channel compared to the conventional case, which shows the dependency between the decrease in this potential and high-k layer parameters. The shift in the potential profile screens the region near the source end from the variations in drain voltage and thus ensures reduction in threshold voltage roll-off in comparison with conventional DG MOSFETs. Thus, gate stack oxide acts as a controlling gate oxide. Second, the surface potential for both structures with traps deviates considerably from that of the fresh device where the potential surface in the damaged subregion is increased when the interface charges N_f are present. This is due to the important effect of the hot-carrier induced localized charge density on the electrons transport characteristics (drain current) through the channel.

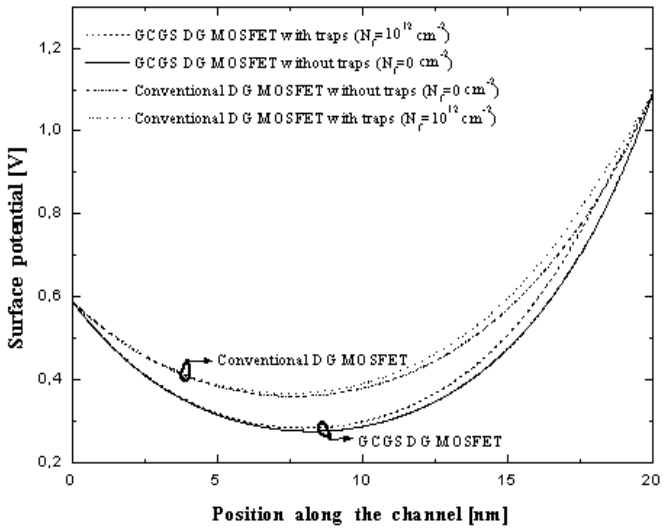


Fig. III.2. Surface potential for Conventional and GCGS DG MOSFET with and without traps ((L_1=L/2, L_d=L/8).

Figure.III.3. compares the threshold voltage roll-off curves as established using our analytical model for the conventional and GCGS DG MOSFET, hot-carrier effects for both structures on the threshold voltage roll-off is also studied (N_f =0 cm^{-2} corresponds to the fresh device and N_f = 10^{12} cm^{-2} to the damaged device). It can be noted that the threshold voltage roll-off increases rapidly as the channel length augments to reach the ideal value when *L >30 nm*.

What is significant is that the discrepancy of curves associated with each prototype becomes more apparent for very short channel length devices (less than 30 nm), which can be explained by the fact that the hot-carrier degradation effect contributes essentially in the

nanoscale domain. The curves deposition confirms that the GCGS DG MOSFET with or without traps has a higher threshold voltage as compared to conventional DG MOSFET.

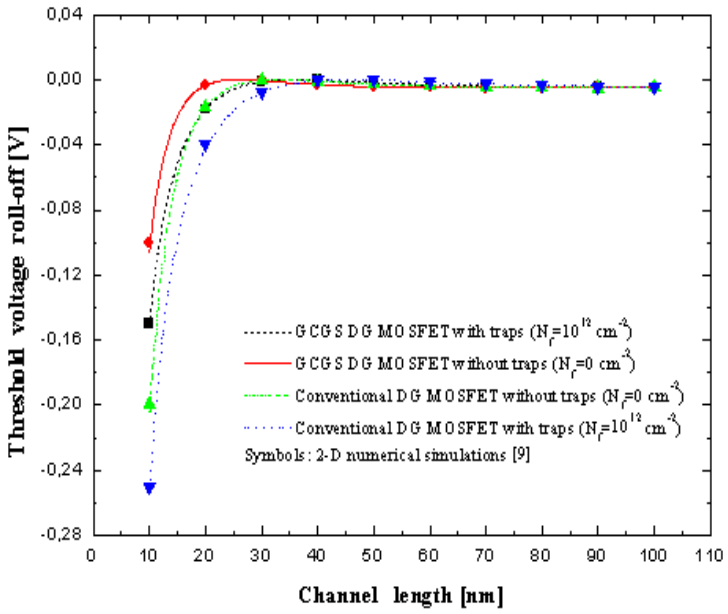


Fig.III.3. Calculated threshold voltage roll-off for Conventional and GCGS DG MOSFET with and without traps (L_1=$L/2$, L_d=$L/3$).

The Drain Induced Barrier Lowering (DIBL), is obtained from the difference between the threshold voltage at high drain-drain source voltage (0.5 V) and the threshold voltage value at low drain-drain source voltage value (0.1 V). As shown in Figure.4, it's clear that DIBL takes its lowest values on curves belonging to GCGS DG MOSFET design without and with traps, while the conventional structure served as a reference indicates an improvement of short-channel-effects provided by the incorporation of graded channel and high-k layer. The DIBL effect is more pronounced in short channel lengths devices, however for very short lengths each type of DG MOSFET (Conventional and GCGS) with and without traps converges to a common point (250 for GCGS and 475 for Conventional DG MOSFET). It is also observed that the DIBL remains unaffected due to the hot carrier density for channel length $L > 30$ *nm*.

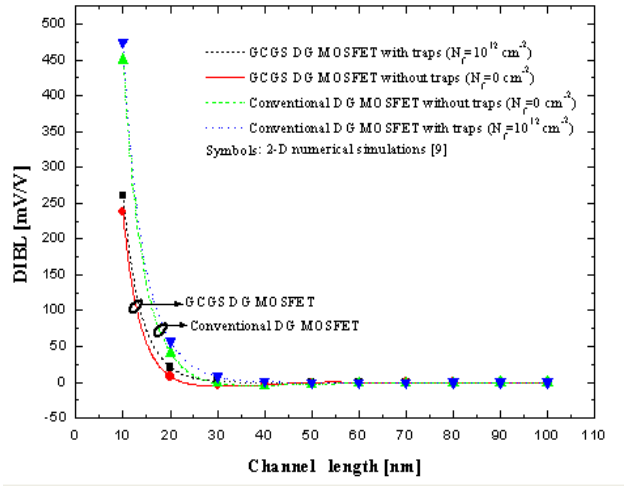


Fig.III.4. Variation of DIBL for Conventional and GCGS DG MOSFET with and without traps as function of channel length (L_1=$L/2$, L_d=$L/3$).

Figure.III.5, shows the variation of subthreshold current as a function of gate voltage. Comparison of both considered prototypes of DG MOSFETs (GCGS and Conventional) with presence and absence of traps, indicates that the GCGS DG MOSFET structure exhibits better performances in term of immunity against the hot-carrier degradation effect, where the OFF-state current for conventional DG MOSFET with traps have been found to be no longer negligible and contribute to standby power where the ratio I_{on}/I_{off} calculated in this case equal to 1.11×10^{7}. Moreover, due to the augmentation of the ratio I_{on}/I_{off} in the case of GCGS DG MOSFET with traps, where the ratio increased to 2.3×10^{9}, our proposed structure satisfies well requirements of high quality commutation from OFF-state to ON-state needed for building efficient downscaled digital circuits.

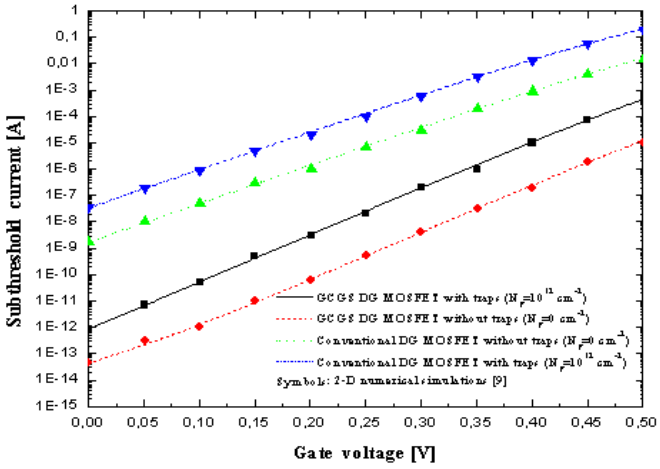


Fig.III.5. Calculated subthreshold current for Conventional and GCGS DG MOSFET with and without traps (L_1=$2L/3$, L_d=$L/6$).

Figure.III.6, plots the subthreshold swing as a function of channel length calculated from our compact model, this is done for conventional and GCGS DG MOFET structures with and without traps. It can be deduced that the subthreshold swing increases rapidly as the channel lengths down and reaches the ideal value for *L >30* nm. The comparison of the subthreshold swing evolution for various cases, shows that the GCGS DG MOSFETs provides better subthreshold swing with or without traps, which is a good indicator validating our assumptions about the immunity of such new structure particularly when compared to conventional devices.

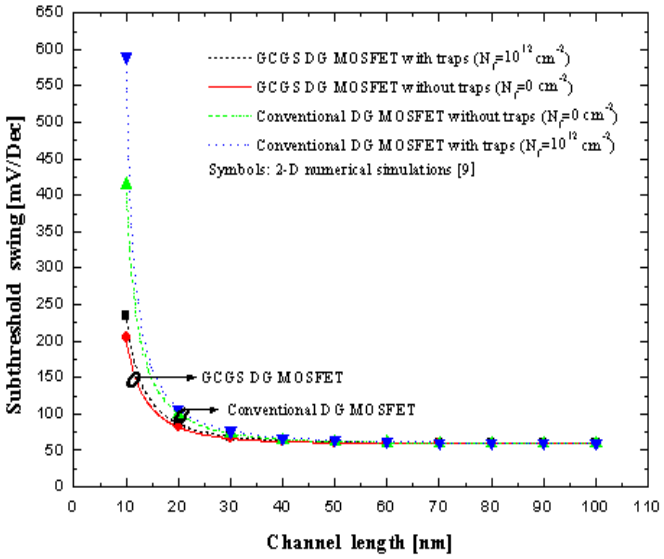


Fig.III.6. Calculated subthreshold swing for Conventional and GCGS DG MOSFET with and without traps as a function of channel length (L_1=*L/2*, L_d=*L/3*).

III.4. CONCLUSION

In this chapter, a two dimensional model which takes into account the hot-carriers degradation effects is used with adequate boundary conditions to investigate the short channel effects, the developed model is dedicated to analyze a new proposed structure, GCGS DG MOSFET, a performance comparison is also carried out by means of conventional DG MOSFET. Based on subthreshold behavior parameters calculation, a considerable improvement was predicted in terms of efficiency and immunity against the presence of an interfacial charge density near the drain side. Hence, the GCGS DG MOSFET device can emerge as one of the promising candidates for reducing the parasitic downscaling resulted effects in low power nano-circuits design.

Chapter IV –

MODELING OF GS DG MOSFET IN LINEAR AND SATURATION REGIONS

***Abstract*:** Due to the excellent control of DG MOSFETs over the short channel effects, they have been considered as a leading candidate to extend the scaling limit of conventional bulk MOSFETs. However, the hot carrier injection into gate oxides remains a potential problem in reliability field hence altering the device lifetime.

In the present chapter, comprehensive drain current models including hot-carrier-induced degradation effects are developed, the derivation is carried out based on some assumptions regarding threshold voltage and mobility. Using obtained models, we have studied the utility of adding a high-k layer into the device structure for which an improvement is detected, the accuracy and efficiency make our analytic current-voltage models for DG MOSFETs suitable for circuit simulation programs.

IV.1. INTRODUCTION

The ongoing downscaling of the bulk technology has resulted in an increase in the transistor count and chip sizes. Thus, new structures have been proposed to scale down CMOS technology more aggressively, among these non classical structures, double-gate (DG) MOSFETs are becoming intense subject of very large scale integration research because of their good performances in suppressing effectively short channel effects, and in this respect, they are an ideal candidate to enable further dimension miniaturization in deep submicron level [47]. In the last years, many approaches for analytic drain current modelling have been elaborated, despite the abundance of such literature surveys, the number of models incorporating the hot carrier degradation effect is very limited up to our knowledge and the development of unified compact models allowing the comparison of different structures based on a common framework is an urgent need. The importance of the considered effect is issued from its impact on several parameters widely used in circuit design field [48].

In this chapter, we introduce three analytic drain current models which are suitable for GS DG MOSFETs. First, the structure under study is presented in section IV.2. Section IV.3. is devoted to the followed steps for the development of the proposed approaches of modeling. Obtained simulation results of the considered structure in term of immunity against hot carrier degradation provided by our analytical expressions are illustrated in section IV.4. Finally, some concluding remarks are highlighted aiming to open new directions on the light of the study particularly in integrated circuit design.

IV.2. DESCRIPTION OF THE STUDIED STRUCTURE

Figure. IV.1. shows the schematic cross-sectional view of a symmetric DG structure considered in this study. To calculate the hot-carrier-damaged drain current we assume that the spatial distribution of hot-carrier-induced negative oxide trapping charge density N_f ($\cong 10^{12} cm^{-2}$) with a length of $L_d = L - L_1$, where L represents the channel length and L_1 is the fresh region length. N_A and $N_{D/S}$ are the doping level of the channel and the drain/source ($\cong 10^{20} cm^{-3}$) regions, respectively. The studied device is assumed to have a width noted by W. The silicon channel thickness and permittivity of the DG MOSFET structure are denoted by t_{si} and ε_{si} respectively, the intrinsic silicon density n_i is taken ($\cong 1.45\times10^{10} cm^{-3}$). The effective oxide layer thickness of insulator layer t_{oxeff} is calculated by combining the thickness

of the SiO_2 layer t_1 with permittivity ε_1 $(=3.9)$ and the thickness of the high-k layer t_2 having permittivity ε_2 $(=10)$ as follows:

$$t_{oxeff} = t_1 + (\varepsilon_1 / \varepsilon_2) t_2 \qquad (IV.1)$$

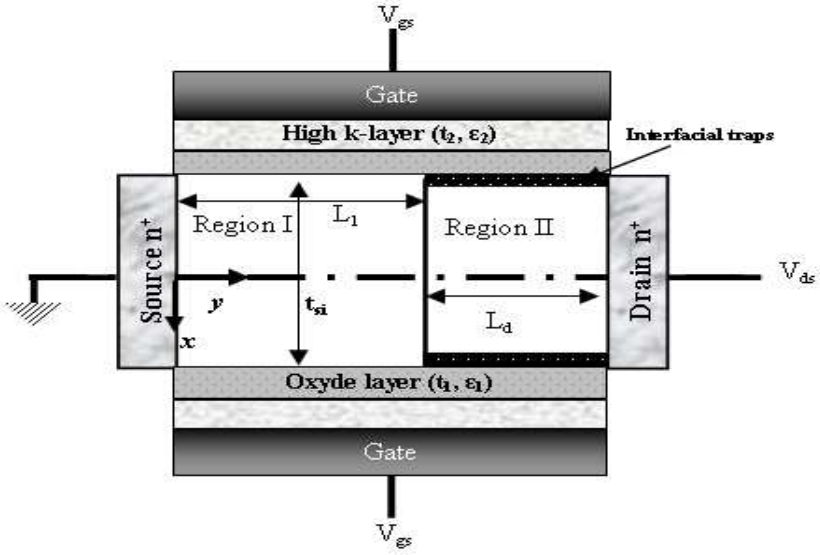


Fig. IV.1. GS DG MOSFET investigated in this work, where region II is the region with hot-carrier induced interface charges.

When the device is operating in or near the saturation region, the electrons moving from the source to the drain experience a significant velocity increase caused by the high horizontal electric field. Such situation is basically responsible about the hot-carrier injection into the gate oxide near the drain side. Although it is quite clear that the hot-carrier-induced oxide charge is localized very close to the drain, the shape of the charge distribution profile is not known exactly and many shapes have been proposed [49-51].

For the derivation of analytical models, we consider the localized oxide-interface charge arising from hot-carrier injection to have a uniform charge profile as:

$$Q_{it}(y) = \begin{cases} 0 & 0 \le y \le L_1 \\ Q_f = qN_f & L_1 \le y \le L \end{cases} \qquad (IV.2)$$

As a result of the uniform charge profile, two device parameters are basically altered; first, the flat-band voltage is augmented by an additional term in damaged region reflecting the hot-carrier degradation effect:

$$V_{fb}(y)=\begin{cases} V_{fb_1}=\Phi_{MS}-\dfrac{Q_{ox}}{C_{ox}} & 0\le y\le L_1 \\ V_{fb_2}=\Phi_{MS}-\dfrac{Q_{ox}}{C_{ox}}-\dfrac{Q_f}{C_{ox}} & L_1\le y\le L \end{cases} \quad \text{(IV.3)}$$

where Φ_{MS} represents the work function difference, Q_{ox} represents the constant positive oxide-interface charge density independent of hot-carrier injection.

The second affected parameter concerns the channel electron mobility, where we have a reduction law represented by Mathiessen's rule in the damaged region [52]:

$$\mu_n(y)=\begin{cases} \mu_{n1}=\mu_0 & 0\le y\le L_1 \\ \mu_{n2}=\dfrac{\mu_0\mu_{ox}}{\mu_0+\mu_{ox}} & L_1\le y\le L \end{cases} \quad \text{(IV.4)}$$

with μ_0 represents the bulk mobility, and $\mu_{ox}=1000\left(\frac{3\times10^3}{N_{it}}\right)\times\left(\frac{T}{80}\right)$ is the oxide-interface charge scattering mobility. The mobility model in device simulation is an important parameter that greatly affects the calculation results [53, 54]. Once we have all these ingredients in hand, the compact model of drain current and small signal parameters can be elaborated in the linear and saturation regions.

IV.3. PROPOSED MODELS FORMULATION

IV.3.1. Piece-Wise Drain Current Models

first model

In linear region and without loss of generality, both considered devices can basically be perceived as two subdevices connected in series each having its own threshold voltage V_{th} and channel length. So, in order to get a compact model, individual drain currents are obtained in the damaged and fresh regions using the charge density in each part and finally an expression for drain current in linear region is obtained that takes into account the presence of interface traps.

The mobile electron charge along the channel region is expressed using the charge-sheet approximation:

$$Q_n(y)=-C_{ox}\left[V_{gs}-V(y)-V_{fb}(y)-2|\Phi_P|\right]+\left[2\varepsilon_{Si}qN_A\left(2|\Phi_P|+V(y)-V_{bi}\right)\right]^{\frac{1}{2}} \quad \text{(IV.5)}$$

Here V_{gs} represents the gate voltage, and Φ_p is silicon barrier potential.

When the DG MOSFET is operating in the linear region, an incremental length, *dy*, along the channel sustains a voltage drop, dV, that can be expressed as the well-known product of the drain current, I_{ds}, and the incremental channel resistance:

$$dV(y) = -I_{ds}\frac{dy}{W\mu_n(y)Q_n(y)} \tag{IV.6}$$

or

$$I_{ds}dy = -W\mu_n(y)Q_n(y)dV(y) \tag{IV.7}$$

The drain current, defined as a positive quantity, is obtained integrating the total current density over the cross-sectional area of the channel. For the fresh region, we have:

$$I_{ds}\int_0^{L_1} dy = -\int_0^W\int_0^{V_p}\mu_n(y)Q_n(y)dVdz \tag{IV.8}$$

where V is the channel voltage.

Integration of equation (IV.8) is straightforward and consideration of the symmetry of the structure, lead for the fresh region (undamaged) to the result:

$$I_{ds} = \frac{2W\mu_{n1}C_{ox}}{L_1}\times\left\{\left(V_{gs}-V_{fb_1}-2|\Phi_P|\right)V_P - \frac{V_P^2}{2} - \frac{2}{3}\frac{\sqrt{2\varepsilon_{Si}qN_A}}{C_{ox}}\times\left[\left(2|\Phi_P|-V_{bi}+V_P\right)^{\frac{3}{2}} - \left(2|\Phi_P|-V_{bi}\right)^{\frac{3}{2}}\right]\right\} \tag{IV.9}$$

By repeating the above calculations for the damaged region with appropriate modifications, a compact analytical drain current model for damaged region can be given as:

$$I_{ds} = \frac{2W\mu_{n2}C_{ox}}{(L-L_1)}\left\{\left(V_{gs}-V_{fb_2}-2|\Phi_P|\right)(V_{ds}-V_P) - \frac{\left(V_{ds}^2-V_P^2\right)}{2} - \frac{2}{3}\frac{\sqrt{2\varepsilon_{Si}qN_A}}{C_{ox}}\times\left[\left(2|\Phi_P|-V_{bi}+V_{ds}\right)^{\frac{3}{2}} - \left(2|\Phi_P|-V_{bi}+V_P\right)^{\frac{3}{2}}\right]\right\} \tag{IV.10}$$

In (IV.9) and (IV.10), V_p represents the channel voltage at the boundary of the damaged region ($y=L_1$). It is easily seen that (IV.9) corresponds to the exact drain current equation of an undamaged transistor with channel length L_1 and drain voltage V_p. Since a damaged DG MOSFET can be considered as two elementary transistors, fresh and damaged regions, having different properties and connected in series, we can get the boundary voltage value, V_p, by equating both expressions of drain current (IV.9 and IV.10) then resolving the nonlinear resulted equation numerically, so that the compact model can be well defined.

In the linear region, it is assumed that an inversion layer exists along the channel from the source to drain, which is true beyond the threshold and for small drain voltages. However, when the drain voltage reaches a certain value the inversion charge at the drain end drops to zero. That is, the channel is pinched-off near the drain end, the drain voltage that results in the disappearance of the channel is referred to as the saturation voltage, and the corresponding current is approximately constant. The expression of the saturation voltage is obtained by either one of these two conditions mathematically equivalent:

$$\left(Q_n(L)=0\right)\Leftrightarrow\left(\frac{\partial I_{ds}}{\partial V_{ds}}=0\right) \tag{IV.11}$$

From equations (IV.5) and (IV.11), an analytical model of the saturation drain voltage can be given as follows:

$$V_{dsat}=V_{gs}-V_{fb2}-2\left|\Phi_P\right|+\frac{\varepsilon_{Si}qN_A}{C_{ox}^2}\left\{1-\sqrt{1+\frac{2C_{ox}^2}{\varepsilon_{Si}qN_A}\left(V_{gs}-V_{fb2}-V_{bi}\right)}\right\} \tag{IV.12}$$

In the damaged GS DG MOSFET model presented here, the channel-end voltage beyond saturation is calculated by taking into account the uniform oxide charge distribution given in (IV.2) and the advantages provided by the DG MOSFET design for long channel devices. Thus, contrary to the conventional bulk MOSFET transistor in saturation, the channel-end voltage does remain equal to V_{dsat}. For $V_{ds}>V_{dsat}$, the saturation drain current of the transistor is found by solving (IV.9) and (IV.10), where the drain voltage in the equations is replaced by the saturation voltage V_{dsat}.

The Small-signal parameters particularly g_m and g_{ds} are required basically for analog circuits design [55]. These parameters can easily be derived from the device drain current models.

Transconductance of a device represents the amplification delivered by the device and is given as:

$$g_m=\left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=cons\tan t} \tag{IV.13}$$

On differentiating (IV.9) with V_{gs}, the expression for transconductance in linear region is obtained as:

$$g_m=\frac{2W\mu_{n1}C_{ox}}{L_1}\left\{V_P+\left(V_{gs}-V_{fb_1}-2\left|\Phi_P\right|\right)\frac{\partial V_P}{\partial V_{gs}}-V_P\frac{\partial V_P}{\partial V_{gs}}-\frac{3r}{2}\left[\left(2\left|\Phi_P\right|-V_{bi}+V_P\right)^{\frac{1}{2}}\frac{\partial V_P}{\partial V_{gs}}\right]\right\} \tag{IV.14}$$

with $r=\dfrac{\sqrt{2\varepsilon_{Si}qN_A}}{C_{ox}}$

$$\frac{\partial V_P}{\partial V_{gs}}=\frac{\left(\dfrac{\mu_{n1}}{L_1}+\dfrac{\mu_{n2}}{L-L_1}\right)C_{ox}WV_P-\dfrac{W}{L-L_1}\mu_{n2}C_{ox}V_{ds}}{\dfrac{W\mu_{n2}C_{ox}}{L-L_1}\left[V_P-\left(V_{gs}-V_{fb_2}-2\left|\Phi_P\right|\right)+\dfrac{3r}{2}\left(2\left|\Phi_P\right|-V_{bi}+V_P\right)^{\frac{1}{2}}\right]-\\ \dfrac{W\mu_{n1}C_{ox}}{L_1}\left[\left(V_{gs}-V_{fb_1}-2\left|\Phi_P\right|\right)-V_P-\dfrac{3r}{2}\left(2\left|\Phi_P\right|-V_{bi}+V_P\right)^{\frac{1}{2}}\right]}$$

The ratio of change in the drain current to the change in the drain voltage is called output conductance and in a similar manner to above calculation we have:

$$g_{ds}=\left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}}=\frac{2W\mu_{n1}C_{ox}}{L_1}\left\{\left(V_{gs}-V_{fb_1}-2\left|\Phi_P\right|\right)\frac{\partial V_P}{\partial V_{ds}}-V_P\frac{\partial V_P}{\partial V_{ds}}-\frac{3r}{2}\left[\left(2\left|\Phi_P\right|-V_{bi}+V_P\right)^{\frac{1}{2}}\frac{\partial V_P}{\partial V_{ds}}\right]\right\} \quad \text{(IV.15)}$$

second model

The expression of threshold voltage resulted from the incorporation of the precedent flat-band voltage is in good agreement with the fact the interface traps leads to an increase in the threshold voltage, the detailed expression of the threshold voltage [56] is given below as:

$$V_{th}(y)=\begin{cases}\phi_{MS}-\dfrac{Q_{ox}}{C_{ox}}+2\phi_B+\dfrac{qN_A\lambda^2}{\varepsilon_{si}} & 0\le y\le L_1\\ \phi_{MS}-\dfrac{Q_{ox}}{C_{ox}}-\dfrac{Q_f}{C_{ox}}+2\phi_B+\dfrac{qN_A\lambda^2}{\varepsilon_{si}} & L_1\le y\le L\end{cases} \quad \text{(IV.16)}$$

However, the threshold voltage of the whole device can be taken as the maximum due to the increase law which means a less sensibility hence reflecting the degradation process:

$$V_{th}=\max_{i=1,2}(V_{thi}) \quad \text{(IV.17)}$$

The modification of the channel electron mobility due to hot-carrier-effects can be modeled using Mathiessen's law as indicated in (IV.4).

In strong inversion region, the inversion charge $Q_n(y)$ at a point z in the channel is given as:

$$Q_n(y)=-C_{ox}\left(V_{gs}-V_{th}(y)-V(y)\right) \quad \text{(IV.18)}$$

Since the drain current is predominantly given by the drift tendency and can be expressed as:

$$I_{ds}=C_{ox}W\mu(y)\left(V_{gs}-V_{th}(y)-V(y)\right)\frac{dV(y)}{dy} \quad \text{(IV.19)}$$

where $dV(y)/dy$ denotes the channel electric field.

The solution of such equation can be found in two adjacent channel regions, by integrating both sides of (IV.19) from the source to the boundary of the damaged region L_1 then from the boundary to the drain, valid expressions of drain current in these regions are carried out as follows:

$$I_{ds}\int_0^{L_1}dy=C_{ox}W\mu_0\int_0^{V_p}\left(V_{gs}-V_{th1}-V(y)\right)dV(y)\Rightarrow I_{ds}=\frac{C_{ox}W\mu_0}{L_1}\left[\left(V_{gs}-V_{th1}\right)V_p-\frac{V_p^2}{2}\right] \quad \text{(IV.20)}$$

$$I_{ds}\int_{L_1}^{L} dy = \frac{C_{ox}W\mu_0\mu_{ox}}{(\mu_0+\mu_{ox})(L-L_1)}\int_{V_p}^{V_{ds}}(V_{gs}-V_{th2}-V(y))dV(y) \Rightarrow$$
$$I_{ds} = \frac{C_{ox}W\mu_0\mu_{ox}}{(\mu_0+\mu_{ox})(L-L_1)}\left\{\left[(V_{gs}-V_{th2})V_{ds}-\frac{V_{ds}^2}{2}\right]-\left[(V_{gs}-V_{th2})V_p-\frac{V_p^2}{2}\right]\right\} \quad \text{(IV.21)}$$

The complete description of the drain current requires the determination of the voltage at the boundary V_p, by equating equations we get the following second order degree equation dealing only with the boundary voltage:

$$\alpha V_p^2 + \beta V_p + \delta = 0 \quad \text{(IV.22)}$$

with

$$\alpha = -\left[\frac{\mu_{ox}}{2(\mu_0+\mu_{ox})(L-L_1)}+\frac{1}{2L_1}\right]$$

$$\beta = \left[\frac{\left(V_{gs}-\phi_{MS}-\frac{Q_{ox}}{C_{ox}}+2\phi_B+\frac{qN_A\lambda^2}{\varepsilon_{si}}\right)}{L_1}+\frac{\mu_{ox}\left(V_{gs}-\phi_{MS}-\frac{Q_{ox}}{C_{ox}}-\frac{Q_f}{C_{ox}}+2\phi_B+\frac{qN_A\lambda^2}{\varepsilon_{si}}\right)}{(\mu_0+\mu_{ox})(L-L_1)}\right]$$

$$\delta = -\frac{\mu_{ox}}{(\mu_0+\mu_{ox})(L-L_1)}\left[\left(V_{gs}-\phi_{MS}-\frac{Q_{ox}}{C_{ox}}-\frac{Q_f}{C_{ox}}+2\phi_B+\frac{qN_A\lambda^2}{\varepsilon_{si}}\right)V_{ds}-\frac{V_{ds}^2}{2}\right]$$

The correct solution of the equation is selected using the familiar quadratic formula in addition to the elementary condition ($0 \le V_p \le V_{ds}$) and is given by:

$$V_p = \frac{-\beta-\sqrt{\beta^2-4\alpha\delta}}{2\alpha} \quad \textbf{(IV.23)}$$

The saturation voltage expression is obtained using (IV.18) to yield:

$$Q_n(L)=0 \Rightarrow V_{dsat} = V_{gs}-\phi_{MS}-\frac{Q_{ox}}{C_{ox}}-\frac{Q_f}{C_{ox}}-2\phi_B-\frac{qN_A\lambda^2}{\varepsilon_{si}} \quad \text{(IV.24)}$$

We can deduce a closed form for small-signal parameters particularly g_m and g_{ds} using equation (IV.20) as follow:

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}} = \frac{C_{ox}W\mu_0}{L_1}\left[V_p+(V_{gs}-V_{th1})\frac{\partial V_p}{\partial V_{gs}}-V_p\frac{\partial V_p}{\partial V_{gs}}\right] \quad \text{(IV.25)}$$

$$g_{ds} = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}} = \frac{C_{ox}W\mu_0}{L_1}\left[(V_{gs}-V_{th1})\frac{\partial V_p}{\partial V_{ds}}-V_p\frac{\partial V_p}{\partial V_{ds}}\right] \quad \text{(IV.26)}$$

Both partial derivatives $\frac{\partial V_p}{\partial V_{gs}}$ and $\frac{\partial V_p}{\partial V_{ds}}$ can be easily obtained from the analytical expression of V_p given in (IV.23).

IV.3.2. Surface potential based drain current model

In this final model, we propose a global analytical approach for obtaining the characteristics of the GS DG MOSFET including hot-carrier degradation effects, based on closed-form solutions of Poisson's and current continuity equations. The model has three distinctive features:

1) The device channel is assumed to be undoped (lightly doped) instead of the usual high channel doping density. Such absence of dopant atoms in the channel further reduces the mobility degradation by eliminating impurity scattering and avoiding random microscopic dopant fluctuations.

2) The analytic drain current model covers all three regions of MOSFET operations: subthreshold, linear, and saturation, thus maintaining strong continuity between different regions, without the need for adjustable parameters which are in general meaningless physically.

3) The compact model for GS DG MOSFET including hot-carrier degradation effect is derived based on the Pao-Sah integral without the charge sheet approximation, so that the volume inversion phenomenon in the subthreshold region can be properly predicted.

Our proposed long-channel model is ideally suitable for being the kernel of an GS DG MOSFET including hot-carrier effects compact formulation. For a complete compact model, this long-channel core would need to be enhanced with additional physical effects, such as short-channel and quantum mechanical effects.

We consider the symmetric GS DG undoped n-channel MOSFET including the hot-carrier degradation effects illustrated in Fig. IV.1. We also consider a long channel enough in order that the device electrostatics is described by 1-D Poisson's equation in the direction vertical to the channel. Neglecting the hole density, Poisson's equation in the silicon is given by:

$$\frac{d^2\psi(x)}{dx^2} = \frac{d^2(\psi(x)-V)}{dx^2} = \frac{qn_i}{\varepsilon_{si}} e^{q\left(\frac{\psi(x)-V}{kT}\right)} \qquad \text{(IV.27)}$$

where q being the electronic charge, n_i the intrinsic carrier concentration, ε_{si} the permittivity of silicon, $\psi(x)$ the silicon band bending, and V the electron quasi-Fermi potential.

Since the current mainly flows along the y-direction, we assume that V is constant along the x-direction; i.e., $V=V(y)$. this is the so called gradual channel approximation. Equation (IV.27)

can then be integrated twice to yield the solution [57]:

$$\psi(x) = V - \frac{2kT}{q}\ln\left[\frac{t_{si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\cos\left(\frac{2\beta x}{t_{si}}\right)\right] \tag{IV.28}$$

The constant β is related to ψ through the boundary condition deduced from Gauss's law:

$$\varepsilon_{ox}\frac{V_{gs} - \Delta\phi - \psi\left(x = \pm\frac{t_{si}}{2}\right)}{t_{oxeff}} = \pm\varepsilon_{si}\left.\frac{d\psi(x)}{dx}\right|_{x=\pm\frac{t_{si}}{2}} \tag{IV.29}$$

Here ΔØ is the work function of both the top and bottom gate electrodes with respect to the intrinsic silicon.

By substituting (IV.28) into (IV.29), we get a nonlinear equation relating β explicitly to different basic parameters:

$$\frac{2\varepsilon_{si}t_{oxeff}}{\varepsilon_{ox}t_{si}}\beta\tan\beta - \ln[\cos\beta] + \ln\beta = \frac{q(V_{gs} - \Delta\phi - V)}{2kT} - \ln\left[\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right] \tag{IV.30}$$

The hot-carrier-induced oxide-interface charge has a significant influence on two device properties: (i) it affects the local electric potential in the adjacent drain region, and (ii) it changes the local channel electron mobility. The potential effect can be accounted for as an additional term in the total mobile charge per unit gate area Q_{inv} in the damaged region. By using (IV.28) combined with $\frac{Q_{inv}}{\varepsilon_{si}} = 2\left.\frac{d\psi(x)}{dx}\right|_{x=\frac{t_{si}}{2}}$, required quantity Q_{inv} expressed in terms of β yields for each region:

$$Q_{inv}(\beta) = \begin{cases} \frac{8\varepsilon_{si}}{t_{si}}\frac{kT}{q}\beta\tan\beta & (0 \le y \le L_1) \\ \frac{8\varepsilon_{si}}{t_{si}}\frac{kT}{q}\beta\tan\beta - 2qN_f & (L_1 \le y \le L) \end{cases} \tag{IV.31}$$

The reduction of channel electron mobility can be represented by Mathiessen's rule as proposed in (IV.4).

For a given V_{gs}, β can be solved from (IV.30) as a function of V. Note that V varies from the source to the drain, the functional dependence of $V(y)$ and $\beta(y)$ is determined by the current continuity equation, which requires the current I_{ds} given by $I_{ds} = \mu W Q_{inv} dV/dy = \mu W Q_{inv}(dV/d\beta)(d\beta/dy)$ to be constant, independent of V or y. The parameter μ is the effective mobility, and W is the device width. Note that dV/dβ can also be expressed as a function of β by differentiating (IV.30) to get:

$$\frac{dV}{d\beta} = -\frac{2kT}{q}\left[\frac{1}{\beta} + \tan\beta + 2\frac{\varepsilon_{si}t_{oxeff}}{\varepsilon_{ox}t_{si}}\frac{d}{d\beta}(\beta\tan\beta)\right] \tag{IV.32}$$

The solution of Pao–Sah's integral can be found in two adjacent channel regions, by integrating both sides of the continuity equation from the source to the boundary of the damaged region L_1 then from the boundary to the drain, valid expressions of the drain current in these regions are carried out as follows: for the fresh region we have:

$$I_{ds} = \mu_1 \frac{W}{L_1} \int_0^{V_p} Q_{inv}(V) dV = \mu_1 \frac{W}{L_1} \int_{\beta_s}^{\beta_p} Q_{inv}(\beta) \frac{dV}{d\beta} d\beta \tag{IV.33}$$

Substituting different factors in (IV.33) and carrying out the integration analytically:

$$I_{ds} = \mu_1 \frac{4W\varepsilon_{si}}{t_{si} L_1} \left(\frac{2kT}{q} \right)^2 \left[\beta \tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si} t_{oxeff}}{\varepsilon_{ox} t_{si}} (\beta \tan\beta)^2 \right]_{\beta_p}^{\beta_s} \tag{IV.34}$$

and for the damaged region:

$$I_{ds} = \mu_2 \frac{W}{L_d} \int_{V_p}^{V_{ds}} Q_{inv}(V) dV = \mu_2 \frac{W}{L_d} \int_{\beta_p}^{\beta_d} Q_{inv}(\beta) \frac{dV}{d\beta} d\beta \tag{IV.35}$$

Substituting appropriate parameters as previously then carrying out the integration analytically yields:

$$\begin{aligned} I_{ds} = {} & \mu_2 \frac{4W\varepsilon_{si}}{t_{si} L_d} \left(\frac{2kT}{q} \right)^2 \left[\beta \tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si} t_{oxeff}}{\varepsilon_{ox} t_{si}} (\beta \tan\beta)^2 \right]_{\beta_d}^{\beta_p} \\ & - \mu_2 \frac{4WN_f kT}{L_d} \left[\ln\left(\frac{\beta}{\cos\beta} \right) + \frac{2\varepsilon_{si} t_{oxeff}}{\varepsilon_{ox} t_{si}} (\beta \tan\beta) \right]_{\beta_d}^{\beta_p} \end{aligned} \tag{IV.36}$$

To compute the drain current we define the following two functions representing the right-hand side of (IV.30) and (IV.34):

$$f_r(\beta) = 2r\beta \tan\beta - \ln[\cos\beta] + \ln\beta \tag{IV.37}$$

$$g_r(\beta) = \beta \tan\beta - \frac{\beta^2}{2} + r(\beta \tan\beta)^2 \tag{IV.38}$$

Note that the range of β is 0< β <π/2 and r is a structural parameter defined as $r = \varepsilon_{si} t_{oxeff} / \varepsilon_{ox} t_{si}$. For given V_{gs} and V_{ds}, β_s and β_d are calculated from the condition (IV.30):

$$f_r(\beta_s) = (q / 2kT)(V_{gs} - V_0) \tag{IV.39}$$

$$f_r(\beta_d) = (q / 2kT)(V_{gs} - V_0 - V_{ds}) \tag{IV.40}$$

where $V_0 = \Delta\phi + \frac{2kT}{q} \ln\left[\frac{2}{t_{si}} \sqrt{\frac{2\varepsilon_{si} kT}{q^2 n_i}} \right]$

At this level, β_p can be also obtained numerically by equating drain current expressions of both damaged and fresh regions.

In the limit case of a fresh device, we have all parameters correspond to those of the fresh region, hence $\beta_p \rightarrow \beta_d$, and as a result our compact model reduces to the drain current model

established in [58]:

$$I_{ds} = \mu_1 \frac{4W\varepsilon_{si}}{t_{si}L}\left(\frac{2kT}{q}\right)^2\left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{oxeff}}{\varepsilon_{ox}t_{si}}(\beta\tan\beta)^2\right]_{\beta_d}^{\beta_s} \quad \text{(IV.41)}$$

Here we have in hand all ingredients required for the elaboration of the drain current model by taking into account the hot-carrier degradation effects. Then, we can write:

$$I_{ds} \alpha \left[g_r(\beta_s) - g_r(\beta_p)\right] \quad \text{(IV.42)}$$

Some asymptotic values and dominance rules regarding different operation modes are summarized in Table. IV.1. [59-60]

TABLE .IV.1. Asymptotic values and dominance rules for different regions of operation.

		$f_r(\beta_s)$	$f_r(\beta_p)$	β_s	β_p	$g_r(\beta_s)$	$g_r(\beta_p)$
Regime	Subthreshold	<<-1	<<-1	~1	~1	/	/
		$\ln\beta_s$	$\ln\beta_p$	/	/	$\beta_s^2/2$	$\beta_p^2/2$
	Linear	>>1	>>1	~ π/2	~π/2	/	/
		$\beta_s\tan\beta_s$	$\beta_p\tan\beta_p$	/	/	$(\beta_s\tan\beta_s)^2$	$(\beta_p\tan\beta_p)^2$
	Saturation	>>1	<<-1	~ π/2	<<1	/	/
		$\beta_s\tan\beta_s$	$\ln\beta_p$	/	/	$(\beta_s\tan\beta_s)^2$	$\beta_p^2/2$

In the following, the GS DG MOSFET including hot-carrier effects regions of operation are derived from this continuous analytical model based on approximations given above.

1) Subthreshold Region [61]:

$$I_{ds} = I_{ds1} + I_{ds2} \quad \text{(IV.43)}$$

with $I_{ds1} = \mu_1 \frac{Wt_{si}n_i kT}{L_1} e^{\frac{q(V_{gs}-\Delta\phi)}{kT}}\left(1 - e^{-\frac{qV_p}{kT}}\right)$ and $I_{ds2} = \mu_2 \frac{Wt_{si}n_i kT}{L_d} e^{\frac{q(V_{gs}-\Delta\phi)}{kT}}\left(1 - e^{-\frac{q(V_{ds}-V_p)}{kT}}\right)$

are the subthreshold currents associated with the fresh and damaged regions based on the basic diffusion current [62], $J_n(y) = qD_n \frac{n_{\min}(y)}{L}\left(1 - e^{\frac{V_{ds}}{V_t}}\right)$, where D_n denotes the diffusion constant, and $n_{min}(y)$ is the minimum carriers concentration at a fixed location along the channel. The subthreshold current is proportional to the cross sectional area of the device, but independent of t_{oxeff}, which is a manifestation of "volume inversion" that cannot be

reproduced by standard charge sheet-based *I–V* models.

2) Linear Region Above Threshold [63]:

$$I_{ds} = 2\mu_1 C_{ox} \frac{W}{L_1}\left(V_{gs} - V_{th} - \frac{V_p}{2}\right)V_p \tag{IV.44}$$

where V_{th} is the threshold voltage, and C_{ox} is the oxide capacitance.

3) Saturation Region:

$$I_{ds} = \mu_1 C_{ox} \frac{W}{L_1}\left[\left(V_{gs} - V_{th}\right)^2 - 2r\left(\frac{2kT}{q}\right)^2 e^{\frac{q\left(V_{gs}-V_0-V_p\right)}{kT}}\right] \tag{IV.45}$$

The saturation current depends on $(V_{gs}\text{-}V_{th})^2$, as expected for a MOSFET. The saturation current approaches the saturation value with a difference term exponentially decreasing with V_p, in contrast to common piecewise models in which the current is made to be constant in saturation [64].

Since all precedent expressions of the drain current depends on the voltage at the boundary of both regions V_p rather than the parameters β_p, an implicit formula for V_p can be obtained from the boundary condition (IV.30):

$$V_p = V_{gs} - \Delta\phi - \frac{2kT}{q}\left[\ln\left(\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right) + 2r\beta_p \tan\beta_p - \ln\left(\frac{\cos\beta_p}{\beta_p}\right)\right] \tag{IV.46}$$

IV.4. RESULTS AND DISCUSSION

IV.4.1. Piece-Wise Drain Current Models

first model

Various parameters used in the simulation are summarized in Table .IV.2.

TABLE .IV.2. Values of parameters used in the simulation based on the first model.

Parameter	Value
L	1×10^{-5} cm
L_1	2L/3 cm
W	2×10^{-5} cm
t_{si}	2×10^{-6} cm
t_1	2×10^{-7} cm
t_2	3×10^{-7} cm
N_{ox}	10^{10} cm^{-2}
N_A	1.5×10^{15} cm^{-3}
μ_0	800 $cm^2/V.s$
$Ø_{MS}$	-0.8385 V

The analytical and numerical *I-V* characteristics of DG and GS DG MOSFETs with and without hot-carrier stress are given in Fig. IV.2. It can be seen that GS DG device has higher current as compared to DG device and the analytical results are found to be in close agreement with the simulated results. It is clear that a reduction in the drain current can be observed in the case of damaged devices. This reduction can be explained by the effect of the trapped electrons in damaged region on the drain current density. Moreover, the drain current degradation becomes more apparent when the gate voltage is increased to higher values.

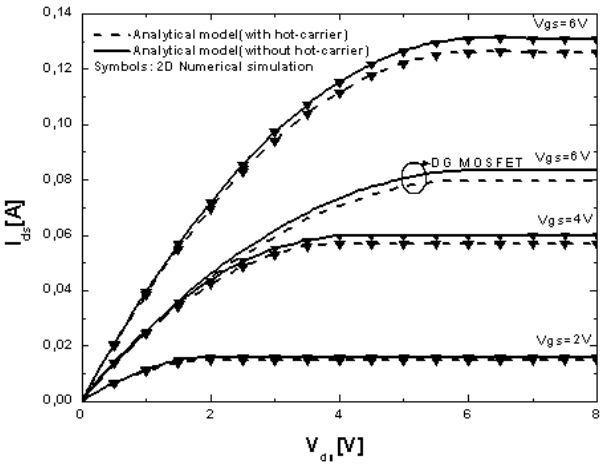


Fig. IV.2. I_{ds}-V_{ds} characteristics for DG and GSDG MOSFETs with and without traps.

The GS DG MOSFET brings prominent advantages in terms of immunity against the hot-carrier degradation effect compared to conventional DG MOSFET. As expected, the threshold voltage increases with the amount of oxide interface charge. This clearly implies that GS DG design leads to a reduction in hot carrier effects and impact ionization and therefore, the hot carrier reliability is considerably improved. Fig. IV.3. shows the advantages of introducing a high-*k* layer on the oxide layer of the DG MOSFET structure when considering the existence of interface traps over the performance of conventional DG MOSFET. As a result of the drop in the biasing voltage of the transistor and the channel carrier mobility, the transconductance also decreases. From this figure, it can be clearly seen that the degradation simulated above threshold value is increasing with increased gate voltage. It is also observed from the figure that GSDG design leads to enhancement in transconductance. A good agreement between analytical and simulated results validates the model.

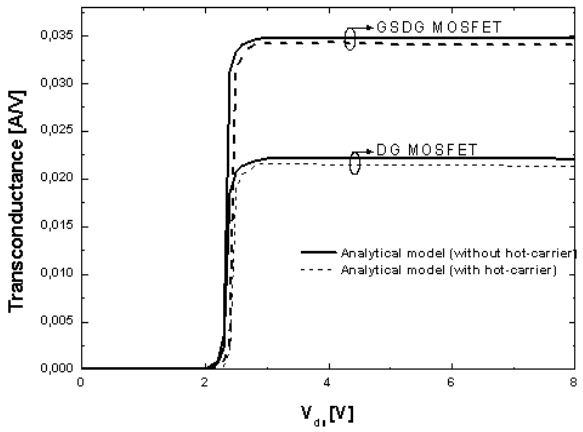


Fig. IV.3. Transconductance variation for both DG and GSDG MOSFETs including hot-carrier effects.

Fig. IV.4. shows the variation of output conductance with drain voltage for both structures including hot-carrier effects. It is observed from the figure that GSDG design leads to enhancement in output conductance for linear region operating mode. In addition, a degradation of the output conductance has been observed for both designs. It is also observed from the figure that the calculated output conductance for the saturation region equal to zero. This result can be explained by the constant value of the drain current in the saturation region (Fig. IV.2.).

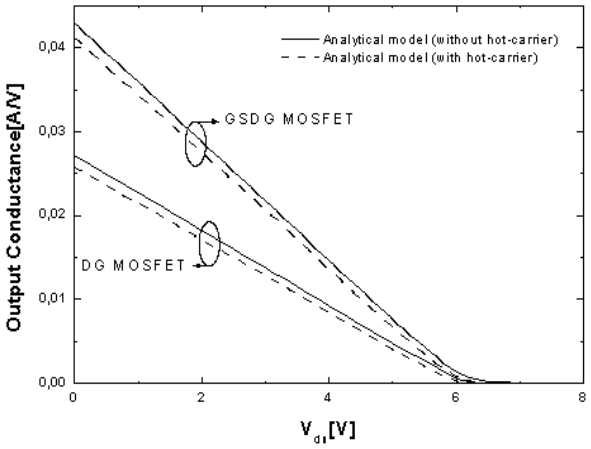


Fig. IV.4. Output conductance versus drain voltage of DG and GSDG MOSFETs.

second model

In order to gain a clear understanding of the behaviour of both structures in response to the presence of an interface charge density near the drain side, the degradation of the main

parameters is studied and the results are presented. All the parameters used in our analysis are given in Table .IV.3.

TABLE .IV.3. Values of parameters used in the simulation based on the second model.

Parameter	**Value**
L	1×10^{-5} cm
L_1	2L/3 cm
W	3×10^{-6} cm
t_{si}	3×10^{-6} cm
t_1	2×10^{-7} cm
t_2	3×10^{-7} cm
N_{ox}	10^{9} cm^{-2}
N_A	10^{15} cm^{-3}
μ_0	800 $cm^2/V.s$
N_f	5×10^{12} cm^{-2}
$Ø_{MS}$	-0.8385 V

As explained in the model formulation, a drop in mobility and an increase of threshold voltage lead to a lower drain current in the device. In Fig. IV.5, a typical diagram I_{ds}-V_{ds} is shown for virgin and damaged DG MOSFETs in both cases with and without high-k layer, where the benefit of including such layer is well proved through the calculation of normalized variation of the drain current $\frac{\Delta I_{ds}}{I_{ds0}}$ as depicted in Fig. IV.6.

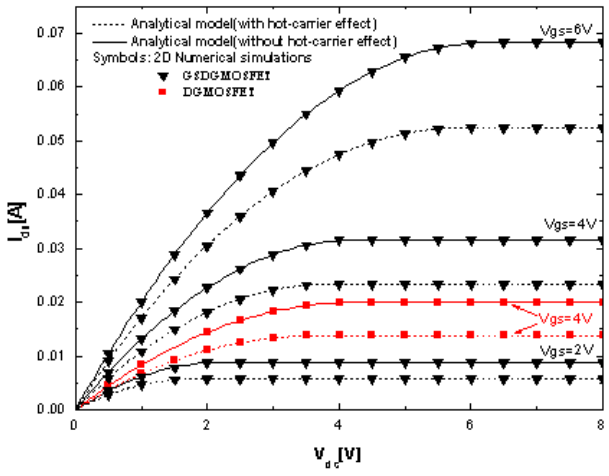


Fig. IV.5. I_{ds}-V_{ds} characteristics of DG MOSFET before and after stress for both cases with and without high-k layer.

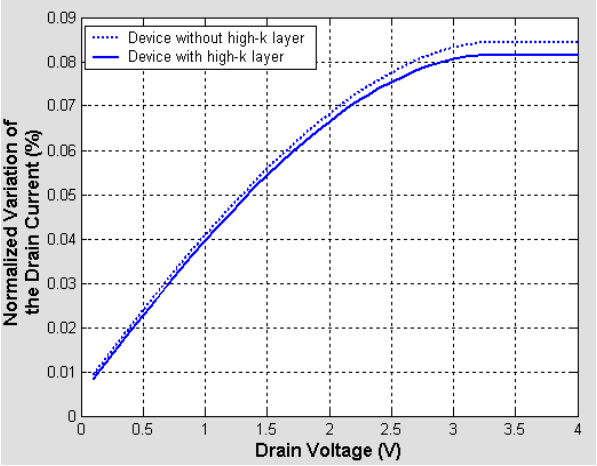


Fig. IV.6. Normalized variation of the drain current of DG MOSFET for both cases with and without high-k layer.

In Fig. IV.7. the calculated drain current degradation versus hot-carrier damage levels, which correspond to different traps densities, is compared with simulation results. The drain current degradation is defined as the decrease of the current at V_{gs}=6V and V_{ds}=8V (saturation regime).

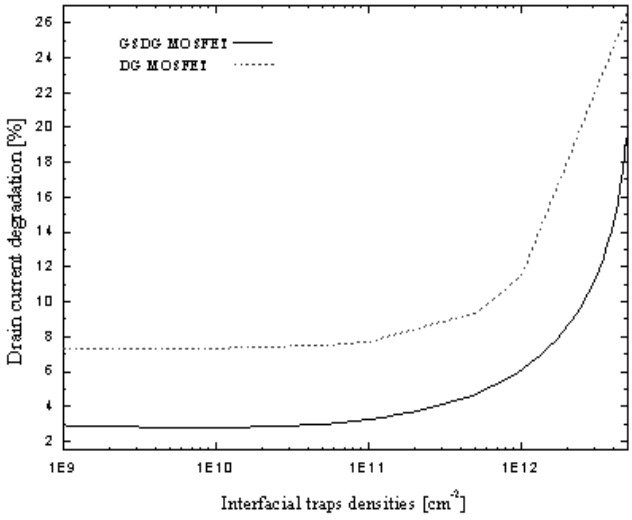


Fig. IV.7. Calculated drain current degradation as function of traps densities for DG MOSFET with high-k layer.

The transconductance degradation for both designs (with and without high-*k* layer) was also plotted in Fig.IV.7. This figure shows a plot of simulated transconductance degradation with respect to the initial transconductance, fresh device, as a function of the traps densities. It can

be noticed that the transconductance decreases as the traps density augments, and reaches a low transconductance values when traps density $N_f > 10^{12}$ cm^{-2} for both cases (GSDG and DG MOSFETs). It is also observed that an improvement, shift in transconductance values, of the transconductance is obtained in the case of GSDG MOSFETs for wide interfacial traps range. Clearly, the GSDG MOSFET design provides better electrical performances and high hot-carrier immunity, with respect to DG MOSFET, in deep submicron domain.

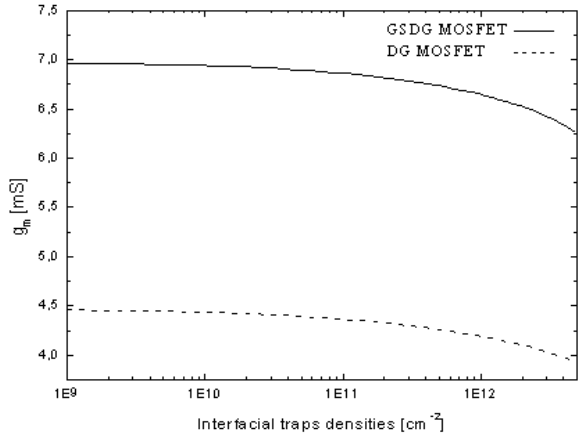


Fig. IV.8. Transconductance degradation as function of interfacial traps densities of DG MOSFET for both cases with and without high-k layer.

IV.4.2. Surface potential based drain current model

Parameters required for the simulation are summarized on the following table:

TABLE .IV.4. Values of parameters used in the simulation based on surface potential model.

Parameter	**Value**
L	2×10^{-5} *cm*
L_1	2L/3 *cm*
W	3×10^{-6} *cm*
t_{si}	2×10^{-6} *cm*
t_1	1×10^{-7} *cm*
t_2	1.5×10^{-7} *cm*
N_A	10^{15} *cm*$^{-3}$
μ_0	800 *cm*^{2}*/V.s*

Figures Fig. IV.9. and Fig. IV.10. show the *I-V* characteristics of DG and GS DG MOSFETs with and without hot-carrier stress. It can be seen that GS DG device has higher current as compared to DG device. It is also clear that a reduction in the drain current can be observed in

the case of damaged devices, this reduction can be explained by the effect of the trapped electrons in damaged region on the drain current density. Moreover, the drain current degradation becomes more apparent when the gate voltage is increased to higher values. The GSDG MOSFET brings prominent advantages in terms of immunity against the hot-carrier degradation effect compared to conventional DG MOSFET, which clearly implies that GS DG design leads to a reduction in hot carrier effects and impact ionization and therefore, the hot carrier reliability is considerably improved.

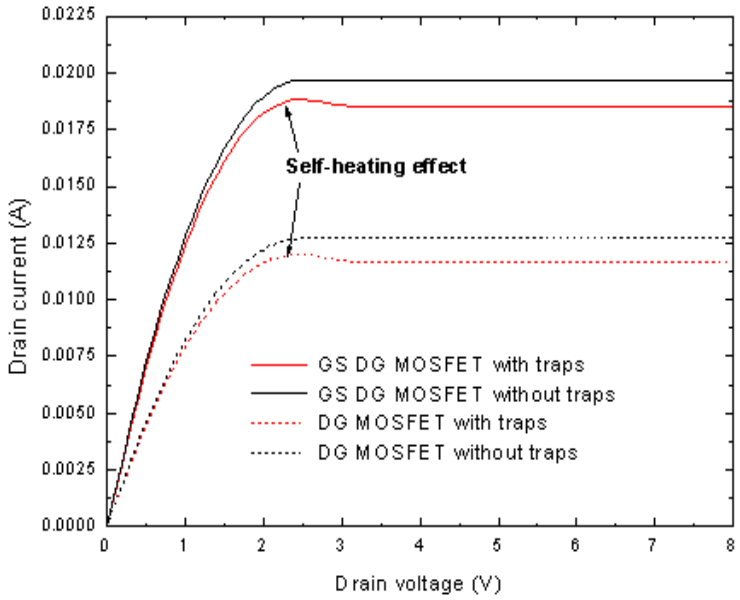


Fig. IV.9. I_{ds}-V_{ds} characteristics of DG MOSFET before and after stress for both cases with and without high-k layer.

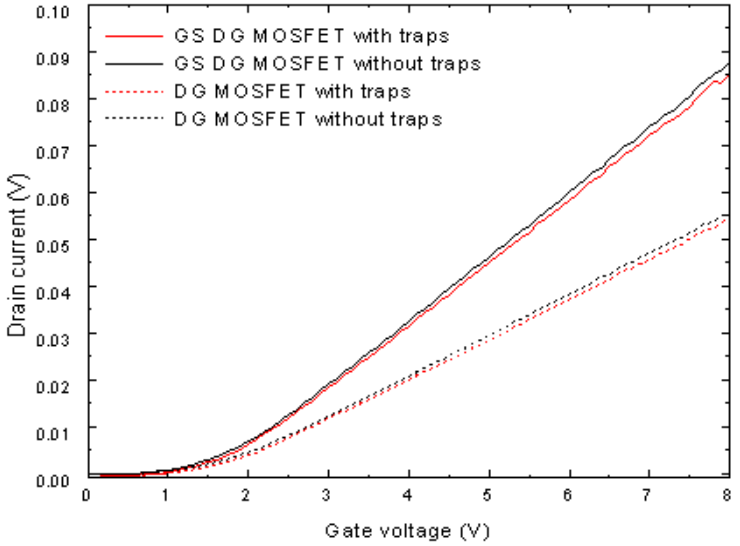
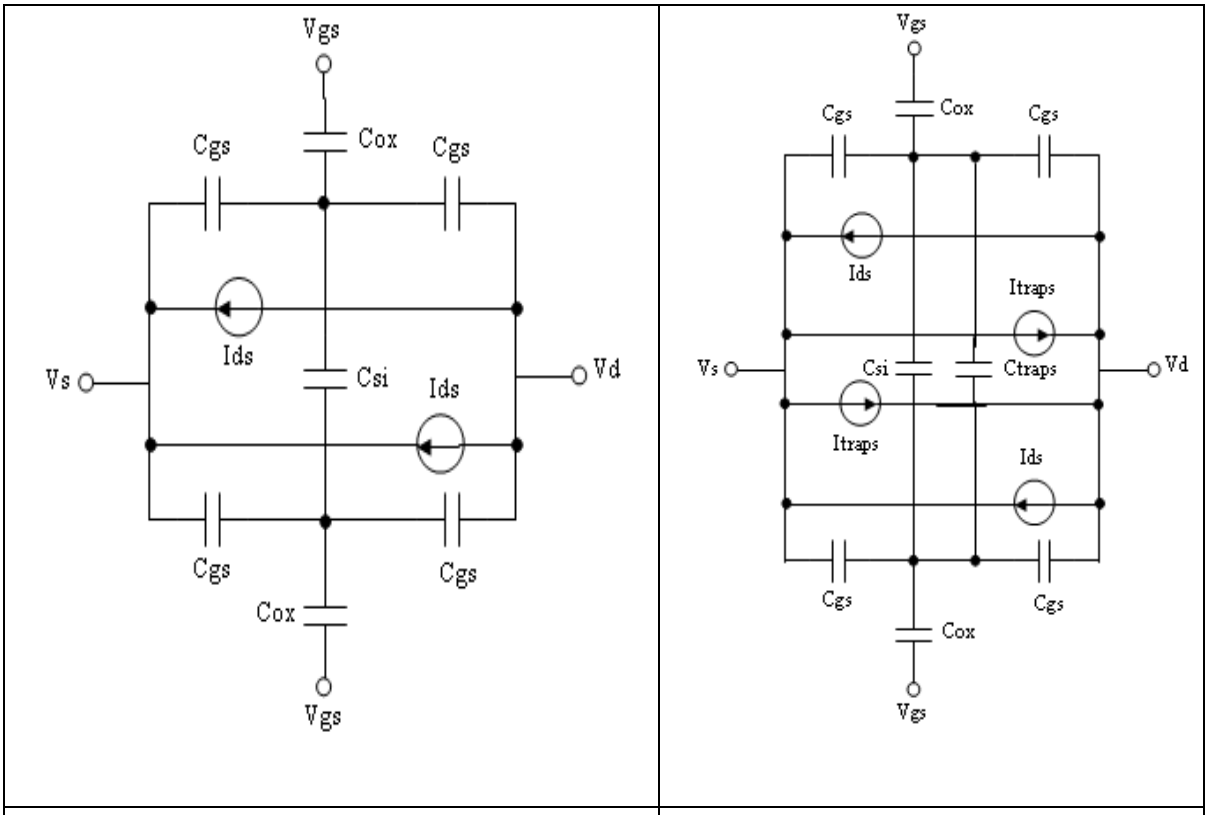


Fig. IV.10. I_{ds}-V_{gs} characteristics of DG MOSFET before and after stress for both cases with and without high-k layer.

IV.5. IMPACT OF HOT-CARRIER DEGRADATION ON IC DESIGN

The existing models of the DG MOSFET in electronic simulators do not take into account the interfacial hot-carrier-induced degradation phenomenon. This latter is purely experimental and very effective in the treatment of the ageing phenomenon. Considering the importance of this phenomenon, we developed a model that is related to the degradation effect. The electric scheme of the DG MOSFET before and after the setting up of the interfacial hot-carrier-induced degradation effect is represented in Fig. IV.11. In this Figure, a new current generators and capacitance which describe the effect of interfacial hot-carrier are clearly presented.



(a) **(b)**

Fig. IV.11. Electric scheme of the GSDG MOSFET without parasitic resistances (*a*) before the implantation of our model, and (*b*) after the implantation of the interfacial hot-carrier degradation effects.

In order to show the impact of our approach on the circuits design, we propose to study the gain and cut-off frequency parameters of a single transistor amplifier under stress conditions as function of traps densities. The amplifier consisted of a GSDG MOSFET and a drain resistance as shown in Fig. IV.12. The drain resistance is set at R_D=2KΩ and the gate voltage is set to give the maximum gain for fresh device. The *(W/L)* ratio of the GSDG MOSFET is

(200/100). The gain and cut-off frequency degradations of a single deep submicron GSDG MOSFET amplifier with traps densities effects are shown in Fig. 6. The initial gain and cut-off frequency, for fresh device without high-*k* layer, are about 8.84 and 528 GHz, respectively. However, the gain and cut-off frequency are degraded to about 7.82 and 455 GHz, respectively, for $N_f = 5.10^{12}\ cm^{-2}$. The gain and cut-off frequency are given by $Gain = g_m / ro$ and $f_T = g_m / 2\pi C_{ox}$, respectively, where ro represents the output conductance of the amplifier, which is considered as constant in saturation region.

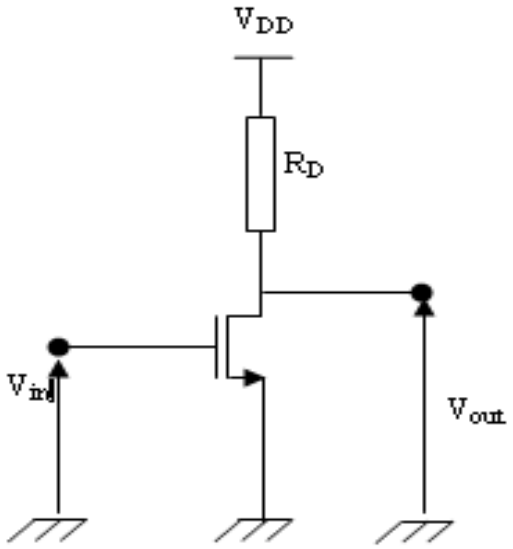


Fig. IV.12. Circuit diagram of a single GSDG MOSFET amplifier.

From Fig. IV.13., it is also observed that an improvement of the gain and the cut-off frequency can be obtained by introducing the high-*k* layer in the device design. To investigate the degradation of the gain and cut-off frequency, the transconductance degradation for both designs (with and without high-*k* layer) was also plotted in Fig. IV.14. This figure shows a plot of simulated transconductance degradation with respect to the initial transconductance, fresh device, as a function of the traps densities. It can be noticed that the transconductance decreases as the traps density augments, and reaches a low transconductance values when traps density $N_f > 10^{12}$ cm^{-2} for both cases (GSDG and DG MOSFETs). It is also observed that an improvement, shift in transconductance values, of the transconductance is obtained in the case of GSDG MOSFETs for wide interfacial traps range. Clearly, the GSDG MOSFET

design provides better electrical performances and high hot-carrier immunity, with respect to DG MOSFET, in deep submicron domain.

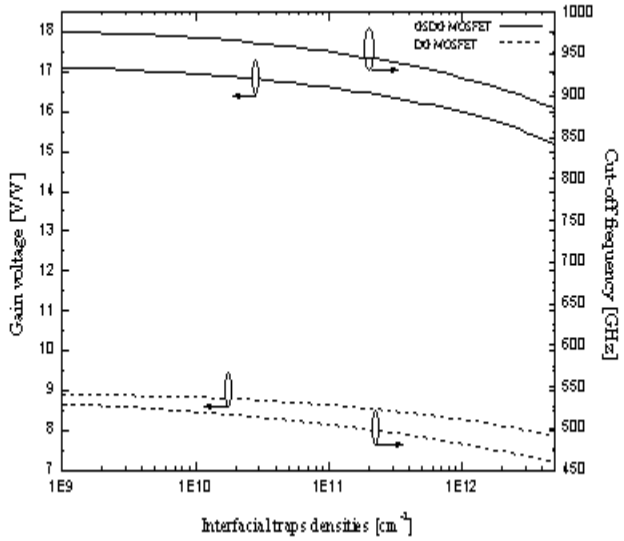


Fig. IV.13. Gain and cut-off frequency degradations of the GSDG MOSFET amplifier as function of interfacial traps densities

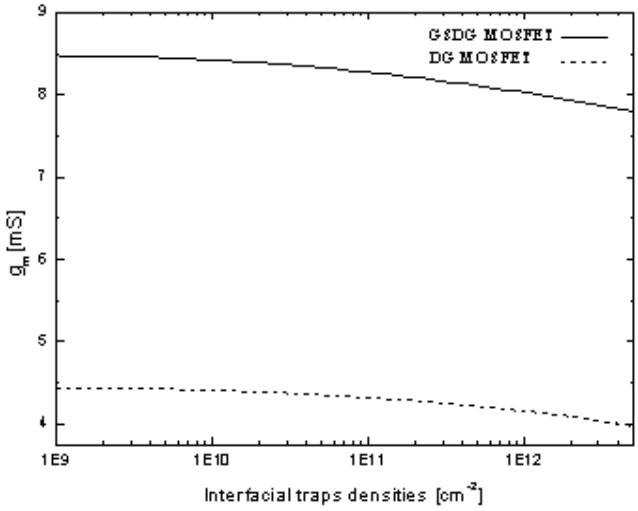


Fig. IV.14. Transconductance degradation as function of interfacial traps densities

IV.6. CONCLUSIONS

This chapter describes compact modeling approaches to study the performances of GS DG MOSFET design including the hot-carrier degradation effects. Based on the development of compact analytical expressions valid in the linear and the saturation regions, the complete behavior scheme of the device including hot-carrier effects can be established. Besides on

providing information about the long term reliability behavior, the compact modeling arguments also help in making a priority order for different prototypes when subject to additional constraints. The elaborated analysis in this chapter is mainly relied on mathematical modeling and assumptions, taking the advantage of the low computational complexity of obtained results without the need of metaheuristics optimization strategies.

CONCLUSION AND FUTURE WORK

Hot-carrier degradation of MOS devices has been considered as a major reliability problem for the past several decades. Empirical and semi-empirical models based on many studies have been used in the past to evaluate the hot-carrier reliability of semiconductor technologies. Some of the most widely used models are based on simplifying assumptions regarding the physical mechanisms responsible for hot-carrier generation, injection and oxide degradation. These assumptions have been known to break down in agreesively scaled semiconductor technologies. In addition, these models are not capable of predicting hot-carrier reliability variations across technologies. Finally, one of the major components that has been missing in past modeling approaches is the ability to model interactions between injected carriers and defects in the oxide.

The hot-carrier modeling approaches presented in this thesis provides a framework to reflect the majority of phenomena occurring in deep submicron MOSFET devices. The use of current-continuity and Poisson's equations allows us to account for the such phenomena in various topologies under study.

Comprehensive models for the drain current in linear and saturation regimes have been developed. This allows us to model the degradation process of the current due to the trapping of injected electrons at defect sites in the oxide. In addition, the change in the small signal parameters caused by injected energetic carriers has been modeled by analytical expressions. One of the most significant additions of this research has been the elaboration of a continuous *I-V* characteristics valid for different regimes of the device function: Subthreshold, linear and saturation regimes, which is to our knowledge done for the first time. The formation of interface traps is the major cause of device degradations due to hot-carrier injection. Using our models, the long-term reliability performance of DG MOSFET structures can be significantly enhanced.

As illustrated in Chapters III and IV, we have successfully modeled hot-carrier degradation of short and long-channel deep submicron MOSFETs using several analytical models. The localized increase of threshold voltage due to trapped electrons in the oxide is shown to result

in an effective channel shortening. This latter affects the channel current as well as the transconductance of the device. Our simulations accurately predict these phenomena.

The different approaches presented here represent a first step towards the technological design process for building hot-carrier reliability in current and future technologies. However, it's possible to undertake some improvements at the level of the mathematical models described to improve the predictability of the modeling approach. Most significantly, an improved model for carrier injection mechanisms across the Si-SiO2 interface is required. The injection model does not account for several physical mechanisms such as carrier tunneling, quantum effects, and interactions with defect levels close to the interface. These physical mechanisms have been identified as some of the key reliability modeling requirements in the ITRS published by SIA and may need to be addressed through a hybrid simulation approach.

The modeling technique used in this research attempts to reduce the use of non-physical empirical or fitting parameters to study the hot-carrier phenomena. While certain key parameters used in our work have to be extracted from a set of experimental data such information may not be available on experimental technologies. In such cases, it might be possible to obtain similar information from other simulation techniques such as commercialized research simulations tools.

Finally, even though the interface-trap model based on a uniform interfacial charge near the drain side close to the interface was sufficient to address the technologies investigated in this thesis, several other profiles such as gaussian and trapezoidal forms have been shown to be of a great help in the handling of various semiconductor device technologies. One or more of these profiles may need to be included in the future to provide a comprehensive set of models for carrier degradation effects in the oxide.

REFERENCES

[1] H. Wong, ″Drain breakdown in submicron MOSFETs: a review,″ Microelectronics Reliability, vol. 40, pp. 3-15, 2000.

[2] K. Hess, L.F. Register, W. McMahon, B. Tuttle, O. Aktas, U. Ravaioli, J.W. Lyding, I.C. Kizilyalli, ″Theory of channel hot-carrier degradation in MOSFETs″, Physica B, no. 272, pp. 527-531, 1999.

[3] P. Masson, J.L. Autran, D. Munteanu, ″DYNAMOS: a numerical MOSFET model including quantum-mechanical and near-interface trap transient effects,″ Solid-State Electronics, vol. 46, pp. 1051–1059, 2002.

[4] ITRS 2007, International Technology Roadmap for semiconductors, Available at <http://www.itrs.com>.

[5] J. Wang, ″Computational Intelligence in Microelectronics Manufacturing,″ Computational Intelligence in Manufacturing Handbook, CRC Press LLC, Boca Raton, USA, 2001.

[6] F. Djeffal, ″Modélisation et Simulation Prédictive du Transistor MOSFET Submicronique,″ PhD dissertation, University of Batna, 2005.

[7] W. Arden, ″Future Semiconductor Material Requirements and Innovations as Projected in the ITRS 2005 Roadmap,″ *Materials Science and Engineering B*, no. 134, pp. 104–108, 2006.

[8] N. Arora, MOSFET Modeling for VLSI Simulation Theory and Practice, International Series on Advances in Solid State Electronics and Technology, World Scientific Publishing, Singapore, 2007.

[9] M. A. Abdi, ″Modélisation de l'Inverse de la Pente sous Seuil des Transistors FETs Nanométriques,″ Msc thesis, University of Batna, 2008.

[10] K. Kurachi, N. Hwang, and L. Forbes, ″Physical Model of Drain Conductance, *gd*, Degradation of NMOSFET's Due to Interface State Generation by Hot Carrier Injection,″ *IEEE Transactions on Electron Devices*, vol. 41, no. 6, pp. 964-969, 1994.

[11] M. P. Pagey, Hot-Carrier Reliability Simulation in Aggressively Scaled MOS Transistors, PhD Dissertation, Electrical Engineering Department, Vanderbilt University, Nashville, Tennessee, USA, Dec. 2003.

[12] K. C. Saraswat, D. Kim, T. Krishnamohan and A. Pethe, ″Performance Limitations of Si Bulk CMOS and Alternatives for Future ULSI,″ *Journal of the Indian Institute of Science*, vol. 87, no. 3, pp. 387-400, 2007.

[13] H. M. Abd-Elhamid, Compact Modeling of Multiple Gate MOS Devices, PhD dissertation, University of Rovira i Virgili, Tarragona-Spain, 2007 .

[14] T. Bentrcia, Y. Tamrabet, E. Belbacha & F. Adjaj, ″Utility of Artificial Intelligence Approaches in the Semiconductor Based Devices Industry: An Overview,″ submitted to *Algerian review of Physics*.

[15] V. H. Geng, Semiconductor manufacturing Handbook, McGraw-Hill, USA, 2005.

[16] M. J. Weber, Handbook of Lasers, CRC Press LLC, 2001.

[17] M. Garey, D. Johnson, Computers and Intractability: A Guide to the Theory of NP-Completeness, W. H.Freeman, San Francisco, CA. 1979.

[18] W. Kuo and M. Zuo, Optimal Reliability Modeling Principles and Applications, John Wiley and Sons, NJ, USA, 2003.

[19] M. P. Pagey, Characterization and Modeling of Hot-Carrier Degradation in Sub-micron NMOSFETS, Msc Thesis, Electrical Engineering Department, Vanderbilt University, Nashville, Tennessee, USA, Aug. 2002.

[20] M. L. Ciurea, V. Iancu, S. Lazanu, A. M. Lepadatu, E. Rusnac, I. Stavarache, ″Defects in Silicon: from Bulk Crystals to Nanostructures,″ *Romanian Reports in Physics*, vol. 60, no. 3, pp. 735–748, 2008.

[21] A. Kuntman, A. Ardali, H. Kuntman and F. Kacar, ″A Weibull Distribution-based New Approach to represent Hot-Carrier Degradation in Threshold Voltage of MOS Transistors,″ *Solid-State Electronics*, vol. 48, pp. 217–223, 2004.

[22] D. Maroudas and S. T. Pantelides, ″Point Defects in Crystalline Silicon, their Migration and their Relation to the Amorphous Phase,″ *Chemical Engineering Science*, vol. 49, no. 17, pp. 3001-3014, 1994.

[23] T. Bentrcia and F. Djeffal, ″Compact Modeling of Multi-Gate MOSFET Including Hot-carrier Effects,″ Chapter 4, CMOS Technology, Series: Electrical Engineering Developments, Editor: Min-jun Kwon, Nova Science Publishers, ISBN: 978-1-61761-325-8, NY, USA, 2010.

[24] E. G. Seebauer and M. C. Kratzer, Charged Semiconductor Defects Structure, Thermodynamics and Diffusion, Springer-Verlag London, 2009.

[25] I. Pintilie, G. Lindstroemb, A. Junkes, E. Fretwurst, ″Radiation-induced Point-and Cluster-related Defects with Strong Impact on Damage Properties of Silicon Detectors,″ *Nuclear Instruments and Methods in Physics Research A*, no. 611, pp. 52–68, 2009.

[26] D. K. Schroder, Semiconductor Material and Device Characterization, Third Edition, John Wiley & Sons, NJ, USA, 2006.

[27] G. P. Karwasz, A. Zecca, R.S. Brusa, D. Pliszka, ″Application of Positron Annihilation Techniques for Semiconductor Studies,″ *Journal of Alloys and Compounds*, no. 382, pp. 244–251, 2004.

[28] Y. Xiaolia, S. Yi, G. Shulin, Z. Jianmin, Z. Youdou, S. Kenichi, I. Hiroki, H. Toshiro, ″Effects of Interface Traps in Silicon-Quantum-Dots-based Memory Structures,″ *Physica E*, vol. 8, pp. 189-193, 2000.

[29] G. La Rosa, S. E. Rauch III, ″Channel Hot-Carrier Effects in n-MOSFET Devices of Advanced Submicron CMOS Technologies,″ *Microelectronics Reliability*, vol. 47, pp. 552–558, 2007.

[30] E. Takeda and N. Suzuki, ″An Empirical Model for Device Degradation Due to Hot-Carrier Injection,″ *IEEE Electron Device Letters*, vol. EDL-4, no. 4, pp. 111-113, 1983.

[31] D. S. Ang, C. H. Ling, ″On the Time-Dependent Degradation of LDD n_MOSFETs under Hot-Carrier stress,″ *Microelectron Reliab*, vol. 39, pp. 1311–1322, 1999.

[32] Y. Leblebici, S-M. Kang, Hot-Carrier Reliability of MOS VLSI Circuits, Dordrecht: Kluwer Academic Publisher; 1993 [chapter 2].

[33] T. Horiuchi, H. Mikoshiba, K. Nakamura, and K. Hamano, ″A Simple Method to Evaluate Device Lifetime Due to Hot-Carrier Effect Under Dynamic Stress,″ *IEEE Electron Device Letters*, vol. EDL-7, no. 6, pp. 337-339, 1986.

[34] C. Hu, S. C. Tam, F-C. Hsu, P-K. Ko, T-Y. Chan, and K. W. Terrill, ″Hot-Electron-Induced MOSFET Degradation-Model, Monitor, and Improvement,″ *IEEE Transactions on Electron Devices*, vol. ED-32, no. 2, pp. 375-384, 1985.

[35] K. R. Mistry and B. Doyle, ″AC Versus DC Hot-Carrier Degradation in n-Channel MOSFET's,″ *IEEE Transactions on Electron Devices*, vol. 40, no. 1, pp.96-104, 1993.

[36] R. Woltjer and G. Paulzen, ″Universal Description of Hot-Carrier-Induced Interface States in NMOSFETs,″ IEDM Technical Digest, pp. 535-538, 1992.

[37] W. Weber and I. Borchert, ″Hot-Hole and Electron Effects in Dynamically Stressed n-MOSFETs,″ in European Solid State Device Research Conference, A. Heuberger, H. Ryssel, and P. Lange, Eds., Berlin, 1989, pp. 719-722, Springer-Verlag, New York.

[38] M. Östling, B.G. Malm, M. von Hartman, J. Hallstedt, Z. Zhang, P. Hellstrom and S. Zhang, ″Challenges for 10nm MOSFET Process Integration,″ *Journal of Telecommunications and Information Technology*, vol. 2, pp. 25-32, 2007.

[39] C. Choi, Modeling of Nanoscale MOSFETS, PhD dissertation, Stanford University, USA, April 2002.

[40] F. Djeffal, M. Meguellati and A. Benhaya, ″A Two-dimensional Analytical Analysis of subthreshold Behavior to study the Scaling Capability of Nanoscale Graded Channel Gate Stack DG MOSFETs,″ *Physica E*, vol. 41, pp. 1872-1877, 2009.

[41] F. Djeffal, Z. Ghoggali, Z. Dibi and N. Lakhdar, ″Analytical Analysis of Nanoscale Multiple Gate MOSFETs Including Effects of Hot-carrier Induced Interface Charges,″ *Microelectronics Reliability*, vol. 49, pp. 377-381, 2009.

[42] K. K. Young, ″Analysis of Conduction in Fully Depleted SOI MOSFETs,″ *IEEE Transactions on Electron Devices*, vol. 36, pp. 504-506, 1989.

[43] M. Fogiel, The Differential Equations Problem Solver, Research and Education Association, NY, 1979.

[44] A. K. Singh, ″An Analytical Study of Hot-carrier Degradation Effects in Submicron MOS Devices,″ *Euro. J. Applied Physics*, vol. 42, pp. 87-94, 2008.

[45] T. Bentrcia**,** F. Djeffal, M.A. Abdi, M. Chahdi & N. Boukhennoufa, ″An Accurate Two Dimensional Threshold Voltage Model for Nanoscale GCGS DG MOSFET Including Traps Effects″, *3rd International Conference on Signals, Circuits and Systems SCS'2009, (CD), pp. 273-277, Djerba, Tunisia, November 06-08, 2009*

[46] A. Dey, A. Chakravorty, N. DasGupta and A. DasGupta, ″Analytical Model of Subthreshold Current and Slope for Asymetric 4-T and 3-T Double-Gate MOSFETs,″ *IEEE Transactions Electron Devices*, vol. 55, pp. 3442–3445, 2008.

[47] O. Moldovan, D. Jiménez, J. R. Guitart, F. A. Chaves and B. Iñiguez, ″Explicit Analytical Charge and Capacitance Models of Undoped Double-Gate MOSFETs,″ *IEEE Transactions on Electron Devices*, vol.54, no. 7, pp. 1718-1724, 2007.

[48] S. Naseh, M. Jamal Deen, C-H. Chen, ″Hot-Carrier Reliability of Submicron NMOSFETs and Integrated NMOS Low Noise Amplifiers,″ *Microelectronics Reliability*, vol. 46, pp. 201-212, 2006.

[49] R. Marrakh and A. Bouhdada, ″Modeling of Interface Defect Distribution for an n-MOSFETs under Hot-Carrier Stressing,″ *Active and Passive Elec., Comp*, vol. 23, 137-144, 2000.

[50] R. Marrakh and A. Bouhdada, ″Modeling of the I–V Characteristics for LDD-nMOSFETs in Relation with Defects Induced by Hot-Carrier Injection,″ *Active and Passive Elec.Comp*, vol. 26, no. 4, pp. 197-204, 2003.

[51] C. J. Sheu and S. L. Jang, ″Modeling of Electron Gate Current and Post-Stress Drain Current of p-type Silicon-on-Insulator MOSFETs,″ *Solide-State Electronics*, vol. 47, pp. 705-711, 2003.

[52] Y. Leblebici, S. M. Kang, ″Modelling of nMOS Transistors for Simulation of Hot-Carrier-Induced Device and Circuit Degradation,″ *IEEE Transactions on Computer-Aided-Design*, vol. 11, no. 2, pp. 235-246, 1992.

[53] F. Djeffal, N. Lakhdar, M. Meguellati and A. Benhaya, ″Particle Swarm Optimization versus Genetic Algorithms to study the Electron Mobility in Wurtzite GaN-based Devices,″ *Solid-State Electronics*, vol. 53, 988-992, 2009.

[54] F. Djeffal, D. Arar, N. Lakhdar, T. Bendib, Z. Dibi, and M. Chahdi, ″An Approach based on Particle Swarm Computation to study the Electron Mobility in Wurtzite GaN,″ *Microelectronics Journal*, vol. 40, 357-359, 2009.

[55] X. Zhou, S. B. Chiah, K. Y. Lim, ″A Compact Deep-Submicron MOSFET g_{ds} Model including Hot-Electron and Thermoelectric Effects,″ *Solid-State Electronics*, vol. 48, pp. 2125–2131, 2004.

[56] F. Djeffal, Z. Ghoggali, Z. Dibi and N. Lakhdar, ″Analytical Analysis of Nanoscale Multiple Gate MOSFETs including Effects of Hot-Carrier induced Interface Charges,″ *Microelectronics Reliability*, vol. 49, pp. 377-381, 2009.

[57] Y. Taur, ″An Analytical Solution to a Double-Gate MOSFET with Undoped Body,″ *IEEE Electron Device Lett.*, vol. 21, pp. 245–247, 2000.

[58] B. Yu, J. Song, Y. Yuan, W. Y. Lu, Y. Taur, ″A Unified Analytic Drain-Current Model for Multiple-Gate MOSFETs,″ *IEEE Transactions on electron devices*, vol. 55, no. 8, pp. 2157-2163, 2008.

[59] Y. Taur, X. Liang, W. Wang,H. Lu, ″A Continuous, Analytic Drain-Current Model for DG MOSFETs,″ *IEEE Electron Device Letters*, vol. 25, no. 2, pp. 107-109, 2004.

[60] D. Jiménez, B. Iñíguez, J. Suñé, L. F. Marsal, J. Pallarès, J. Roig, and D. Flores, ″Continuous Analytic I–V Model for Surrounding-Gate MOSFETs,″ *IEEE Electron Device Letters*, vol. 25, no. 8, pp. 571-573, 2004.

[61] T. Bentrcia, F. Djeffal & D. Arar, ″An Analytical Two Dimensional Subthreshold Current Model for Nanoscale GC GS DG MOSFET Including Interfacial Traps Effects,″ 2nd International Conference on Electronic Systems CISE'2009, pp. 173-177. Batna, Algeria, October 25-26, 2009.

[62] A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, G. Pananakakis and N. Collaert, Analytical modelling for the current–voltage characteristics of undoped or lightly-doped symmetric double-gate MOSFETs, Microelectronic Engineering, vol. 87, no. 9, pp. 1764-1768, 2009.

[63] T. Bentrcia, F. Djeffal, M.A. Abdi & D. Arar, ″A Compact Analytical Current Model including Traps Effects for GS DG MOSFETs,″ Accepted in 2010 XIth International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design SM2ACD'2010, Tunis-Gammarth 05-06 October 2010, Tunisia.

[64] F. Djeffal, T. Bentrcia, and T. Bendib, ″An Analytical Drain Current Model for Undoped GS DG MOSFETs including Interfacial Hot-Carrier Effects,″ Accepted for publication in *Physica Status Solidi*, pssc.201000158, 2010.

Abstract

In recent years, advances in semiconductor manufacturing techniques have driven the associated MOSFET sizes close to their physical limits. The presence of mobile carriers in the oxides triggers the degradation of device and circuit behavior due to injection of energetic carriers from the silicon substrate into the surrounding dielectrics known as “hot-carrier degradation”. This work is dedicated to the compact modeling of proposed nanodevices. The thesis is divided into four chapters, the first one is reserved to the state of the art of multi-gate devices. The second describes the hot-carrier degradation phenomenon. The followed chapter gives the main steps of the analysis of a new device in subthreshold region. Finally, in the last chapter, analytical models for the drain current in linear and saturation regions are presented. We hope that this work has succeed in reaching the fixed goals and satisfying results too.

Keywords: *Hot-carrier degradation effect, multi-gate device, compact analytical modeling.*

Résumé

Dans les dernières années, le développement des techniques de matériaux semi-conducteurs a engendré la réduction de la taille de la structure MOSFET à l’échelle physique. La présence de charge mobile dans l’oxyde déclenche la dégradation des performances de la structure. Le travail abordé dans ce mémoire est consacré à la modélisation compacte des structures nanométriques. Le mémoire est composé de 4 chapitres, le premier est consacré à l’état de l’art de structure multi-grille. Le deuxième décrit le processus de dégradation causé par ces défauts d’interface. Le chapitre suivant donne les étapes de l’analyse d’une nouvelle structure dans le régime sous seuil. On termine par le développement de models analytiques pour le courant du drain dans les régimes linéaire et de saturation. Nous pensons que ce travail a permis d’atteindre les objectifs fixés ainsi que des résultats satisfaisants.

Mots clefs: *Effet de dégradation par les porteurs de charge chauds, structures multi-grilles, modélisation analytique compacte.*

ملخص

في السنوات الأخيرة أدت التطورات في تقنيات صناعة المواد النصف الناقلة إلى بلوغ المركبات الالكترونية أبعادها الحدية الدنيا. إن وجود الشحنات المتحركة في الأكسيد يتسبب في نقصان فعالية الدارة بسبب انتقال الشحنات ذات الطاقة العالية من طبقة السيليسيوم إلى العوازل المحيطة وهو ما يعرف بتأثير الشحنات الساخنة. العمل المقدم في هذه المذكرة يهدف إلى الدراسة و النمذجة التحليلية لبنيات مركبات بأبعاد نانومترية. تحتوي المذكرة على أربعة فصول وخلاصة عامة حيث أن الفصل الأول يهتم بتقديم المركبات المتعددة البوابات. الفصل الثاني يقدم تفسيرا لمختلف الظواهر المترتبة عن فعل الشحنات الساخنة الناتجة عن الشوائب الحدية. الفصل التالي يوضح الخطوات الأساسية لتحليل بنية مقترحة جديدة في المنطقة تحت الحدية. وفي الفصل الأخير تم تطوير عدة نماذج تحليلية للتيار صالحة في كل من المنطقة الخطية و منطقة الإشباع. وفي الأخير نرجو أن العمل المنجز مكن من بلوغ الأهداف المخطط لها.

الكلمات المفتاحية: *تأثير التناقص بفعل الشحنات الساخنة، البنيات متعددة البوابات، النمذجة التحليلية المقلصة.*